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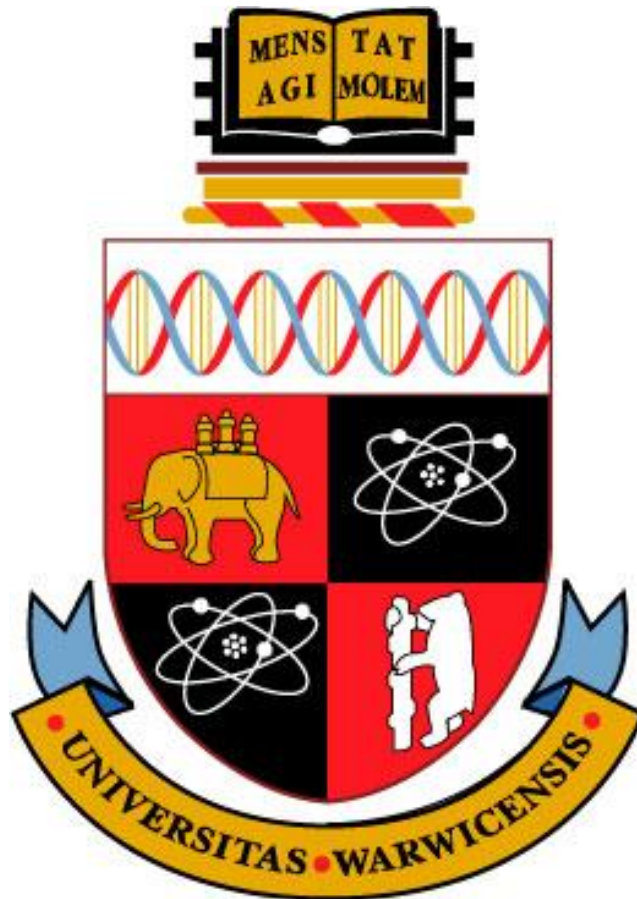
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Development of a Fault Tolerant MOS Field Effect Power Semiconductor Switching Transistor



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Dissertation submitted for the degree of
Doctor of Philosophy
June 2012

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Acknowledgements

Firstly, I would like to thank my PhD supervisor Professor Phil Mawby, who had faith in me to deliver quality research work from the outset, even when I myself had doubts. When I lost faith, or lost my way, then I could always rely on some well placed answers to my questions and indeed get answers to some questions that at the time I did not know I was going to need. Above all I wanted to thank Phil for giving me the space to learn from my own multitudinous mistakes.

I would also like to thank Dr Peter Ward for his straight forward practical approach and whose enthusiasm for the subject of semiconductor devices was contagious.

My thanks also to Dr James Covington who helped me shape this thesis.

I would like to thank Professor Julian Gardner for his timely guidance during the often turbulent duration of this study for PhD; and indeed all the staff and colleagues of the school of engineering who helped make my study time at the University of Warwick enjoyable.

I would like to express my gratitude also to Professor Mark Johnson of the University of Nottingham for his supportive yet probing questioning which prompted the direction of the performance evaluation work. Indeed I would also like to thank Mark Harrington and Adrian Shipley of G.E. Aviation who kept me informed of the needs of the aerospace industry and provided guidance as to the importance and aims of this work.

Finally, I dedicate this work to my family and friends who gave me the strength to continue through extremely challenging times. These people are never far from my thoughts. My Mother proved to be a tower of strength and support throughout. My Father, had he lived to have seen it, would most probably been horrified at my career break choice, but I hope he would have been proud of me in having the flexibility and tenacity to complete this work. To my partner Dr Melanie Pope and our daughter Zara Rose then we proved we can do anything together if we apply ourselves wholeheartedly to it and have faith in the outcome. The true success of this work was that we as a new family learnt to enjoy the journey together in an ever changing world.

“Try not to become a man of success, but a man of value”.
Albert Einstein

Declaration

The author wishes to declare that apart from commonly understood and accepted ideas, or where reference is made to the work of others, the work in this thesis is his own. It has not been submitted in part, or in whole, to any other university for a degree, diploma or other qualification. The work presented in chapter 7 has been published by Westmoreland as shown at Appendix 1, page 271.

Martin Westmoreland.
June 2012

Abstract

This work describes the development of a semiconductor switch to replace an electro-mechanical contactor as used within the electrical power distribution system of the More Electric Aircraft (MEA; a project begun in the 1990's by the United States Air Force). The MEA is safety critical and therefore requires highest reliability components and systems, but subsequent to a short circuit load fault the electro-mechanical contactor switch often welds shut. This risk is increased when using high discharge energy lithium ion dc batteries. Predominately the semiconductor switch controls inductive loads and is required to safely turn off current of up to 10 times the nominal level during sporadic load fault events. The switch requires the lowest static loss (lowest on state resistance), but also the lowest dynamic loss (losses due to the switching event). Presently, unipolar devices provide the lowest dynamic loss, but bipolar devices provide the lowest static loss. One possible solution is use of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET), the area of which is sized to suit the fault current, but at relatively high cost in terms of silicon area. The resultant area is typically achieved by several die connected in parallel, unfortunately, such a solution suffers from current share imbalance and the potential of cascade die failure. The use of a parallel combination of unipolar and bipolar device types (MOSFET and Insulated Gate Bipolar Transistors, IGBTs) to form a hybrid appears to offer the potential to reduce the silicon area, and static loss, whilst reducing the impact of the increased dynamic losses of the IGBT. Unfortunately, this goal requires optimised gate timing of the resultant hybrid which proves challenging if the load current is to be shared appropriately during fault switching in order to prevent failure. Some form of single MOS (Metal Oxide Semiconductor) gated integrated hybrid device with self biased bipolar injection is therefore required to ensure highest reliability through a non latching design which offers lowest losses under all conditions and achieves an even temperature distribution.

In this work the novel concept of the integrated hybrid device has been investigated at a low Blocking Voltage (BV) rating of 100 V, using computer simulation. The three terminal hybrid silicon DMOS (Double diffused Metal Oxide Semiconductor) device utilises a novel merged Schottky p-type injector to provide self biased entry into a reduced static loss bipolar state in the event of high fault current. The device achieves a specific on state resistance, $R_{(ON,SP)} = 1.16 \text{ m}\Omega\text{cm}^2$ in bipolar mode (with $BV=84 \text{ V}$), that is below the silicon limit line and requires half the area of a traditional unipolar MOSFET to conduct fault current. During comparative standard unclamped inductive switching trials, the hybrid device provides a self clamping action which enables increased inductive energy switching (higher inductance and/or higher load current), relative to that achieved by either the MOSFET or IGBT. The hybrid conducting in bipolar mode switches an inductive load off much faster than that typically achieved by an IGBT ($t_{off}=20 \text{ ns}$, in comparison to typically $>10 \mu\text{s}$ for an IGBT). This results in a low turn off energy for the hybrid ($1.26 \times 10^{-4} \text{ J/cm}^2$) as compared to that of the IGBT ($8.72 \times 10^{-3} \text{ J/cm}^2$). The hybrid dynamic performance is enhanced by the action of the merged Schottky contact which, unlike the IGBT, acts to limit the emitter base voltage (V_{EB}) of the internal PNP Bipolar Junction Transistor, BJT (the integral PNP BJT is otherwise a shared feature with the IGBT). The self biased bipolar activation is achieved at a forward bias (V_{AK}) = 1.3 V at temperature (T) = 300 K. The device is latch up free across the operational temperature range of $T=233 \text{ K}$ to 400 K. A viable charge balanced structure to increase the BV rating to approximately 600 V is also proposed.

The resulting performance of the single gated, self biased, hybrid, utilising a novel merged Schottky/P type injector, could lead to a new class of rugged MOS gated power switching devices in silicon and potentially silicon carbide.

Nomenclature

English Alphabet

A	Cross sectional area, or active device area	cm^2
ac	alternating current	
A_{dep}	Anode depletion extent into P-body	cm
BV :	Blocking Voltage	Volts (V)
BV_F :	Forward blocking voltage (anode +ve, V_{AK})	Volts (V)
BV_R :	Reverse blocking voltage (cathode +ve, V_{KA})	Volts (V)
BV_{CEO}	Open base transistor breakdown	Volts (V)
C_{OX}	Oxide capacitance	Farad (F)
C_d	Depletion capacitance	Farad (F)
C_{TOT}	Total gate capacitance	Farad (F)
c_p	Capture co-efficient of holes	$\text{cm}^3 \text{s}^{-1}$
d	Change in magnitude	
dc	direct current	
D_L	Drift length	cm
D_{it}	Density of interface traps (SiO_2 to Si interface)	cm^{-2}
D_p	Diffusivity of holes	cm^2/s
D_n	Diffusivity of electrons	cm^2/s
D_{pB}	Diffusivity of holes in the base region of a BJT	cm^2/s
D_{nE}	Diffusivity of electrons in the emitter of a BJT	cm^2/s
D_V	Vertical unipolar drift length (in lateral hybrid)	cm
E_C	Conduction band energy level	eV
E_G	Energy gap	eV
E_i	Intrinsic energy level	eV
E_{FS}	Fermi level in semiconductor	eV
E_{FM}	Fermi level in metal	eV
E_{FN}	Fermi level in n-type semiconductor	eV
E_{FP}	Fermi level in p-type semiconductor	eV
E_V	Valence band energy level	eV
E_{off}	Turn off energy	Joules
g_{mL}	Transconductance in linear region	Siemens (S)
g_{ms}	Saturation transconductance	Siemens (S)
h_{FB}	Common base gain (α)	
I_A	Anode current	Amps (A)
I_B	Base current	Amps (A)
$I_{A,sat}$	Anode saturation current	Amps (A)
I_C	Collector current	Amps (A)
I_E	Emitter current	Amps (A)
I_K	Cathode current	Amps (A)
I_L	Leakage current	Amps (A)
I_O	Saturation current (P-N junction)	Amps (A)
I_{TE}	Total current for electrons	Amps (A)
I_{TH}	Total current for holes	Amps (A)
$I_{diff,B}$	Diffusion current of holes into the base region	Amps (A)
$I_{diff,E}$	Diffusion current of electrons into the emitter region	Amps (A)
J	Total current density	A/cm^2
J_n	Electron current density	A/cm^2
J_p	Hole current density	A/cm^2
$J_{A,sat}$	Anode saturation current density	A/cm^2
J_L	Leakage current density	A/cm^2
J_{SCG}	Space charge generated current	Amps (A)

J_O	Saturation current density (P-N junction)	A/cm ²
J_{TN}	Current density within the N-Drift region in low injection	A/cm ²
K_{dep}	Cathode depletion extent into P-body	cm
L	Inductance	H
L_n	Minority carrier diffusion length for electrons	cm
L_p	Minority carrier diffusion length for holes	cm
L_{Sub}	Substrate thickness	cm
L_A	Accumulation region length	cm
L_{CH}	Channel length	cm
L_{eff}	Effective channel length	cm
L_{pB}	Minority carrier diffusion length in the base region	cm
N_d	Donor doping concentration	cm ⁻³
N_a	Acceptor doping concentration	cm ⁻³
n_i	Intrinsic carrier concentration	cm ⁻³
n_n	Concentration of electrons in an n-type semiconductor	cm ⁻³
n_p	Concentration of electrons in a p-type semiconductor	cm ⁻³
n_{no}	Concentration of electrons in an n-type semiconductor at equilibrium	cm ⁻³
n_{po}	concentration of electrons in a p-type semiconductor in equilibrium	cm ⁻³
N_C	Effective density of states in the conduction band	cm ⁻³
N_V	Effective density of states in the valence band	cm ⁻³
N_T	Number of recombination centres	cm ⁻³
N_{dB}	Donor concentration in the PNP BJT base region	cm ⁻³
N_{aE}	Acceptor concentration in the PNP BJT base region	cm ⁻³
P	Power	W
P_k	Peak value	
p_n	Concentration of holes in an n-type semiconductor	cm ⁻³
p_p	Concentration of holes in a p-type semiconductor	cm ⁻³
p_{no}	Concentration of holes in an n-type semiconductor at equilibrium	cm ⁻³
p_{po}	Concentration of holes in p type semiconductor at equilibrium	cm ⁻³
Q_S	Total charge in semiconductor	Coulomb (C)
Q	Stored charge in N-Drift region of Schottky	Coulomb (C)
Q_{OX}	Total effective charge in the oxide	Coulomb (C)
R	Resistance	Ω
R_A	Resistance of accumulation region	Ω
r	Radius of curvature (P-body)	cm
R_A	Accumulation resistance in a MOSFET	Ω
R_{CH}	Channel resistance in a MOSFET	Ω
$R_{(ON,SP)}$	Specific on-state resistance	Ωcm^2
$R_{(ON)}$	On state resistance	Ω
R_{VE}	Vertical resistance to electrons	Ω
R_{VH}	Vertical resistance to holes	Ω
R_{SC}	Resistance of the N-Drift between P-Anodes to Schottky	Ω
R_{Sub}	Resistance of Substrate of thickness L_{Sub}	Ω
Sc	Schottky	
t_{OX}	Thickness of the oxide	cm
T	Ambient heat sink temperature	K
t	Time	s
t_{off}	Time to turn off	s
t_{on}	Time to turn on	s

t_{fall}	Gate ramp down time (V_{GK} goes to 0 V)	s
U	Net recombination/generation rate	$\text{cm}^{-3}\text{s}^{-1}$
V_{AK}	Anode to cathode voltage (anode +ve)	Volts (V)
V_{KA}	Cathode to anode voltage (cathode +ve)	Volts (V)
V_{BI}	Built in potential of a semiconductor junction	Volts (V)
V_{GK}	Gate to cathode voltage	Volts (V)
V_{EB}	Emitter to base voltage (emitter +ve)	Volts (V)
V_{BE}	Base to emitter voltage (base +ve)	Volts (V)
V_{EC}	Emitter to collector voltage (emitter +ve)	Volts (V)
V_{FS}	Voltage at which a Schottky diode begins conduction	Volts (V)
V_{FB}	Flat band voltage of the MOS channel	Volts (V)
V_{TH}	Threshold voltage	Volts (V)
V_P	Channel Pinch off voltage	Volts (V)
V_{PT}	Punch through voltage	Volts (V)
$V_{P+to N-}$	Forward voltage across the P-Anode to N-Drift junction	Volts (V)
$V_{N-to N+}$	Forward voltage across the N-Drift to N+ substrate junction	Volts (V)
V_{N-}	Voltage across the N-Drift region	Volts (V)
V_{SC}	Forward voltage drop across the Schottky diode	Volts (V)
W_B	Base width (of a Bipolar Junction Transistor)	cm
W_{B-EFF}	Effective base width (of a Bipolar Junction Transistor)	cm
W_E	Emitter width (of a Bipolar Junction Transistor)	cm
W_{DEB}	Depletion width of base to emitter junction (BJT)	cm
W_D	Depletion width	cm
W_{DMAX}	Maximum depletion width	cm
W_{DMOS}	MOS capacitor depletion width	cm
W_{Dn}	Depletion extent into n-type region of P-N junction	cm
W_{Dns}	Depletion extent into n-type region of Schottky junction	cm
W_{Dp}	Depletion extent into p-type region of P-N junction	cm
W_G	Gate electrode width	cm
W_N	PiN diode intrinsic region drift length ($W_N = W_B$)	cm
X	Lateral dimension	cm
Y	Vertical dimension	cm
Y_{JP}	Depth of P-body to N-Drift metallurgical junction	cm
Y_{N+}	Depth of N+ cathode to P-body metallurgical junction	cm
Z	Cell thickness/ channel width	cm

Greek Alphabet

α	Common base gain (h_{FB})	
α_T	Base transport factor	
β	Common emitter gain (h_{FE})	
γ_s	Injection ratio (Schottky)	
γ	Emitter injection efficiency	
ε_{MAX}	Electric field maximum	V/cm
ε_X	Lateral electric field in MOS channel	V/cm
ε_Y	Perpendicular electric field (to surface) in MOS channel	V/cm
η	Ideality factor (diode)	
λ	Thermal conductivity	W/mK
μ_n	Electron mobility	$\text{cm}^2/\text{V s}$
μ_h	Hole mobility	$\text{cm}^2/\text{V s}$
μ_{ni}	Inversion layer mobility	$\text{cm}^2/\text{V s}$

μ_e	Effective inversion layer mobility	$\text{cm}^2/\text{V s}$
ρ	Resistivity	Ωcm
τ_{sc}	Space charge region carrier lifetime	s
τ_N	Carrier lifetime (electron)	s
τ_P	Carrier lifetime (hole)	s
v	Average drift velocity	cm/s
Φ_{Bn}	Barrier height (Schottky diode)	eV
Φ_M	Metal work function (Schottky contact)	eV
χ_O	Affinity of SiO_2	eV
χ_S	Affinity of Semiconductor	eV
ψ_B	Potential difference between E_i and E_{FS}	eV
ψ_S	Surface potential	eV

Physical constants & material properties

k	Boltzmann constant	$8.6174 * 10^{-5}$	eV/K
q	Electron charge	$1.60218 * 10^{-19}$	C
ϵ_{crit}	Critical electric field (silicon)	$\approx 2\text{-}3 * 10^5$	V/cm
	Critical electric field (SiC)	$\approx 1 * 10^6$	V/cm
	Critical electric field (GaN)	$\approx 5 * 10^6$	V/cm
ϵ_r	Relative permittivity (general form)	$(\epsilon_o * K_{xxx})$	F/cm
ϵ_s	Permittivity of silicon	$1.044 * 10^{-12}$	F/cm
ϵ_{SiC}	Permittivity of SiC	$8.55 * 10^{-13}$	F/cm
ϵ_{GaN}	Permittivity of GaN	$7.8 * 10^{-13}$	F/cm
ϵ_O	Permittivity of free space	$8.854 * 10^{-14}$	F/cm
K_O	Dielectric constant of the SiO_2	3.9	
K_S	Dielectric constant of Silicon	11.8	
K_{SiC}	Dielectric constant of SiC	9.66-9.72	
K_{GaN}	Dielectric constant of GaN	8.9-9.7	
χ_{Si}	Electron affinity of silicon	4.05	eV
A^*	Richardson Constant for silicon	110	$\text{cm}^{-2} \text{K}^{-2}$

Periodic table elements

Symbol	Element name	Group
Ga	Gallium	group III
B	Boron	group III
Al	Aluminium	group III
Ge	Germanium	group IV
Si	Silicon	group IV
C	Carbon	group IV
As	Arsenic	group V
N	Nitrogen	group V
P	Phosphorous	group V
Sb	Antimony	group V
Pt	Platinum	group VIII
O	Oxygen	group VI

General abbreviations

Symbol	Description
BJT	Bipolar Junction Transistor
CB	Contact Breaker (electro-mechanical switch)
DMOS	Double diffused Metal Oxide Semiconductor
ELMC	Electrical Load Management Centre
HVDC	High Voltage Direct Current (electrical power transmission)
IGBT	Insulated Gate Bipolar Transistor
JBS	Junction Barrier Schottky (diode)
MCT	MOS controlled Thyristor
MEA	More Electric Aircraft
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NPT IGBT	Non Punch Through Insulated Gate Bipolar Transistor
PT IGBT	Punch Through Insulated Gate Bipolar Thyristor
SSPC	Solid State Power Controller
UMOS	‘U’ shaped trench Metal Oxide Semiconductor
VDMOSFET	Vertical Double diffused Metal Oxide Semiconductor Field Effect Transistor

Definition

The term ‘Ohmic contact’ within this work means the current–voltage (I-V) curve for the metal semiconductor junction is in the linear region, is symmetrical and non rectifying.

Chapter 1 | Introduction

1.0 Introduction

This chapter introduces the need for power electronic switching devices within the present global community and provides some basic information on what characteristics should be provided by an ideal power switch. An introduction to some of the basic types of voltage controlled switching power semiconductor types will then be made comparing these to the ideal characteristic. The aim of this research work is to provide a semiconductor power switching device for an electrical power distribution application (Solid State Power Controller, SSPC) within the More Electric Aircraft (MEA). In particular the switch in this application requires extremely high reliability hence be tolerant to sudden current increase due, for example, to a short circuit fault in the load. This requirement is particularly acute due to the use of lithium ion energy storage batteries which have extremely high discharge energies if the load is short circuit. The switch not only has to safely conduct this increased current level (say 10 times the nominal load current level), but also reliably switch off from that fault current. In this safety critical aircraft application any switch failure could potentially cause a cascade to catastrophic failure and was to be avoided. The switching device had to provide the lowest possible conduction loss (static loss), but also the lowest dynamic loss to prevent excessive self heating in either state. The requirement therefore was to extend the safe operation area of the semiconductor switching technology, in terms of voltage and current, therefore reducing the risk of the switching device failing for thermal

reasons. This chapter also provides an overview of the thesis which documents the work to achieve the optimised switch design and verification of the device performance.

1.1 Role of power electronics in the global community

The expanding use of power electronics within aircraft is targeted at achieving improved conversion efficiencies. Such efficiency improvements may also be translated into a multitude of uses such as domestic appliances, lighting, computing and industrial motor drives through to transportation and even how the electrical power is distributed to consumers, both industrial and domestic, from the national network of generation. The motivation for the increased usage of power electronics is to gain efficiencies via control of the energy usage. Such accumulated efficiencies on a national level enable reduction or redundancies within the national network of generation at a time when usage of electrical power is escalating. If for example, the power required for national lighting needs is reduced through the majority use of LED (Light Emitting Diode) lighting, the design of which was made possible via power conversion achieved through power electronics, then potentially, through accumulative reduction in UK power demand, a carbon fuelled fired power station could potentially be decommissioned which would reduce CO₂ emissions into the atmosphere and thus help reduce the effects of global warming, as summarised by Drury[1]. Indeed, the need for industrial power drives alone accounted for 60 % of the all the UK electrical energy consumption and the application of power electronics in controlling those led to a 30-40 % reduction in the energy used according to Drury. Due to the widening usage of power conversion the report by Drury on behalf of the U.K government estimated that the global market for power electronics was around £135 billion and growing at a rate of 10 % per annum. Transport applications were currently around 13 % of that total market, but this was potentially the fastest growing market sector for power electronics usage due to the transition to low carbon emission vehicles such as hybrids like the Toyota Prius and ultimately, upon provision of the correct national infrastructure, then totally electric vehicles like the Nissan Leaf represent an achievable low carbon future. This is especially the case if

electrical power generation migrated toward ‘greener’ low carbon sources, such as wind, tide and solar energy. Currently however, it is estimated that by 2035, then 90 % of the available liquid fuel oil would be utilised in passenger transportation, according to the World Energy Council[2].

1.2 Solid state switching devices

The availability of solid state power electronic devices began in 1948 when the point contact germanium transistor was first described by Bardeen and Brattain[3]. The theory of current flow in such junction transistors was described by Shockley[4], wherein the current through the device was controlled via a third terminal, thus forming a variable resistance. Eventually, the development of such solid state devices, as fabricated in relatively low cost silicon, replaced vacuum tubes as the current control device of choice due to an improved cost-performance balance. Since that time many varied device structures have become available in many different types of material; starting with germanium (Ge) and silicon (Si) and more recently compound semiconductor materials such as gallium arsenide (GaAs), gallium nitride (GaN) and silicon carbide (SiC). Each device structure and material gave the switching element a unique characteristic and capability; hence device types and materials were more suited to certain applications than others.

The application considered within this research work is the solid state power controller (SSPC) to be used within the More Electric Aircraft (MEA), to be described later within chapter 2. Typical applications and systems ratings consider both dynamic and static operational states, the SSPC application considered in this thesis is indicated in figure 1.1 relative to other applications as depicted and described by Baliga[5]. For this purposes of this device concept work figure 1.2 defines the area of interest for the static measures of performance shown relative to the silicon limit line, Hu[6]. Although the MEA requirement is $BV=500$ V [7], this work focuses on achieving a low voltage rating conceptual design which, dependent upon current level, is capable of operation both above the silicon limit line (in unipolar mode) and below the silicon limit line in bipolar mode. The lowest loss state

(lowest $R_{(ON,SP)}$) is desired hence the need for bipolar conduction, but the bipolar conduction is known to have a detrimental effect on dynamic losses, due to extended t_{off} times so this is to be a focus of evaluation, especially with consideration to inductive load switching.

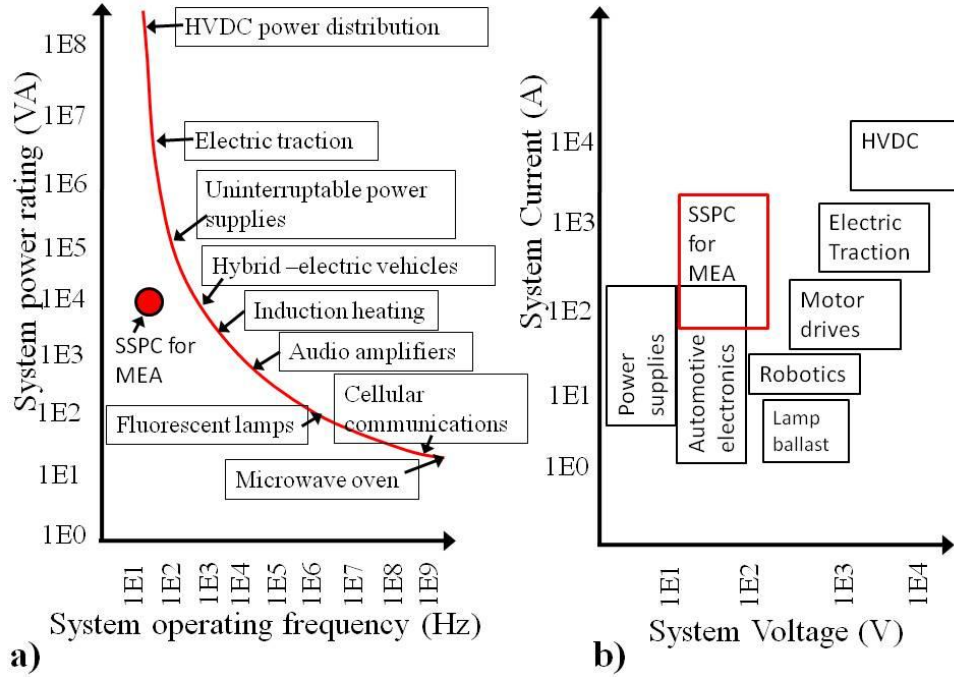


Figure 1.1. Applications and systems ratings for SSPC relative to power electronics for a) dynamic and b) static modes of operation.

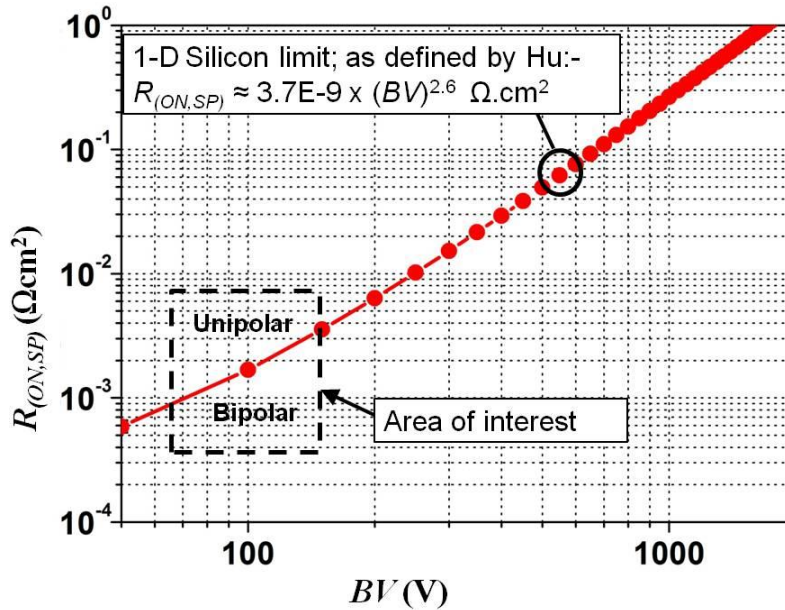


Figure 1.2. Definition of the area of interest for this work in terms of static measures of performance relative to the silicon limit line.

1.3 The ideal power switch characteristics

The ideal switching characteristic is shown in figure 1.3 a) essentially the ideal switch has infinite resistance when in the 'off' state (to an infinite voltage magnitude dropped across the device) and infinite conductivity when in the 'on' state. In addition the transition between states would be completed instantaneously, thus the energy loss during the switch transition period would be very small. Unfortunately, the performance of a typical real switching device is shown in figure 1.3 b). Real devices are unfortunately subject to the development of a forward voltage dropped across them due to a finite resistance when conducting in the 'on' state. The magnitude of the voltage in relation to the current level achieved provides a figure of merit for static loss, where the lowest voltage for highest

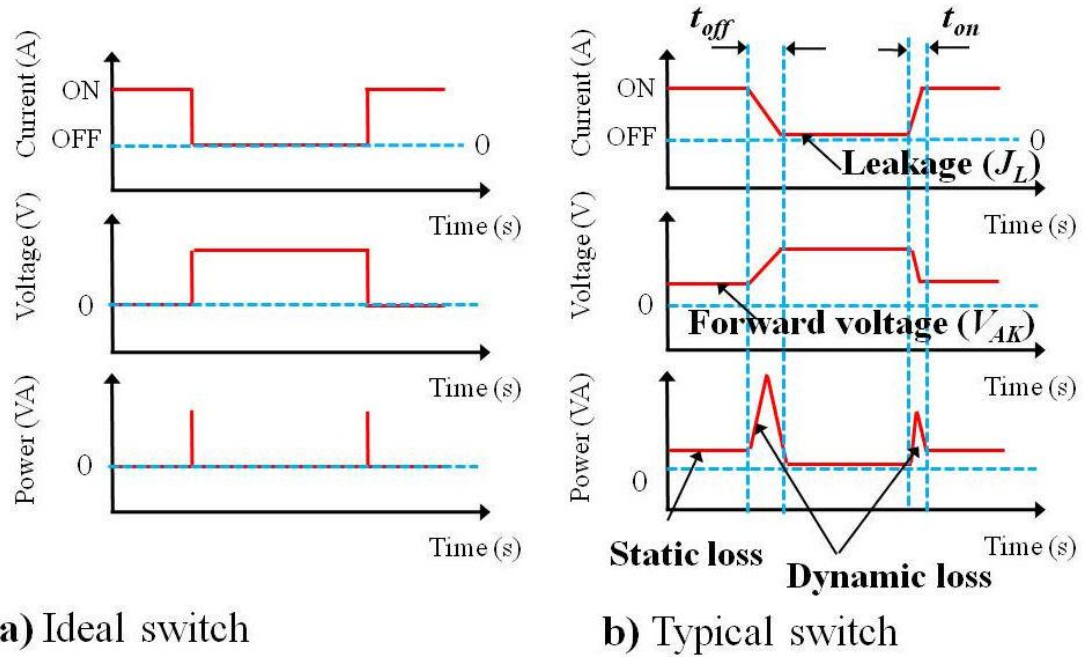


Figure 1.3. Comparison switching characteristics both a) ideal and b) for typical solid state switching.

current is required. This is termed the static, or conduction loss. In addition when in the 'off' state a small leakage current (J_L) can flow, thus galvanic isolation is not possible. Dependent predominantly upon the dielectric constant of the material used within a real device, then it will block a finite level of voltage, but once the blocking voltage (BV) is exceeded the device will once again conduct, termed an avalanche current. The avalanche current at such a high

voltage would cause extremely high power dissipation and self-heating which is clearly undesirable. The largest issue and highest probability failure mode however, is in the transition or switching mode, this is especially true with inductive loads like electric motors as described by Hummert[8]. Hummert described that the inductive load can be thought of as an additive voltage source that simultaneously acts to maintain current flow through itself via the switch once that switch is turned off. The current therefore, continues to flow via the switch resistance, which is steadily increasing as the device progressively turns off. Not only is the current flowing, but also the increased forward voltage appears across the device, thus leading to high power dissipation (where power is the product of volts and amps, $P = V_{AK} I_K$, in units of Watts). In the switch transition any losses, as measured in energy (Joules) or power (Watts), is termed the dynamic loss. The significance of the dynamic loss increases with increased switching frequency. Depending on the transition time, either turn off time (t_{off}), or turn on time (t_{on}) then the total energy loss could potentially be very large causing the self generation of heat which in turn can act to increase the loss through increased voltage, current, or both. Such a situation is called thermal runaway and the device will ultimately expire in a time which is dependent upon the material used. Some materials are better thermal conductors than others and would allow the heat flux to flow into a heat sink at a faster rate, in which case the effect of the transient event may be dissipated more effectively thus preventing thermal failure.

The attributes of the power switching device which determine the suitability to any application are the switching frequency (which determines dynamic losses) and the on state resistance (static losses), both of which tend to increase with blocking voltage rating. The trait of increasing static loss with BV rating is particularly apparent with unipolar device types (which conduct using holes, or electrons, but not both). Bipolar devices (which conduct using both hole and electron carrier types to form a total current) provide the lowest static loss relative to a unipolar device of the same BV rating, but have higher dynamic losses than unipolar devices and so lend themselves to low switching frequency applications. As the switching frequency is increased the use of unipolar devices is therefore required

because these use one type of carrier and hence the recovery to equilibrium from the conducting state is relatively fast, thus they have low dynamic loss. The issue however, is that the static losses in unipolar device structures are dependent upon the mobility of the carriers through the material, thus the selection of the material offering the highest carrier mobility of the selected carrier type (either electrons or holes) is required.

The static (or dc) forward voltage (V_{AK}) and reverse voltage (V_{KA}) characteristics of the predominant types of power switching devices currently available are shown in figure 1.4. Both the predominant types offer voltage controlled conduction via a Metal Oxide Semiconductor (MOS) ‘gate’ which was used to activate a ‘channel’ formed by the electrostatic attraction of electrons in the case of the devices shown in figure 1.4 a) and b) where electrons are attracted to provide controlled conduction via an N-channel. The

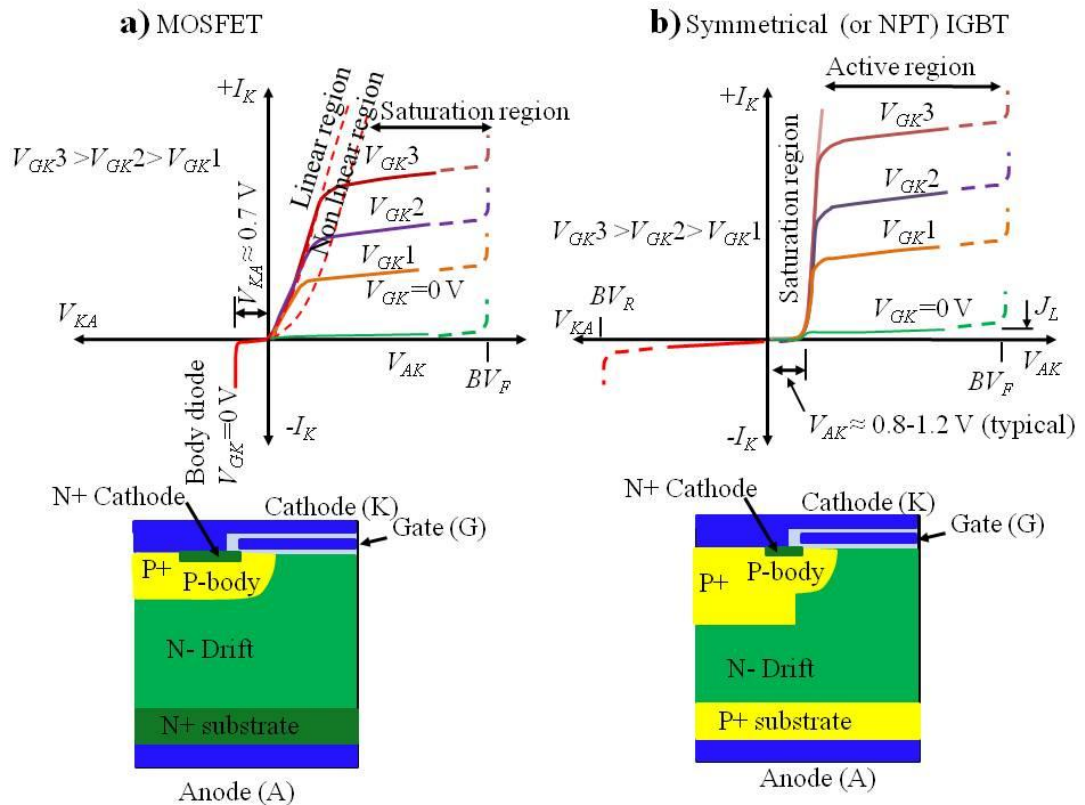


Figure 1.4. Comparison of the static (dc) characteristics of a) a unipolar MOSFET and b) a bipolar Non Punch Through (NPT) IGBT.

predominant types featured are the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), which is a unipolar device utilising electrons, and the Insulated Gate Field

Effect Transistor (IGBT) which is a bipolar device. The MOSFET has low dynamic losses, but the static losses are active area dependant (likened to the effect of resistors connected in parallel), but the IGBT has the lowest static losses due to the bipolar conduction and requires a reduced active area to conduct the same current (at the same voltage) as a larger area unipolar MOSFET.

The aim of this work is to combine the benefits of both the unipolar and bipolar device types to create a hybrid device which ideally has both the low static losses of the IGBT, but also benefits from the low dynamic losses of the MOSFET. What was achieved provided a fast switching device in silicon which benefited from both unipolar and bipolar conduction modes, which meant reduced dynamic losses when compared to an IGBT. Bipolar conduction was achieved via the use of a novel merged Schottky/acceptor (boron) doped anode, which provided a self biased automatic transition from the unipolar to bipolar mode (no gate bias adjustment, or external trigger was required) in the event of an abrupt rise in current demand through the device (such as a load fault). Thus, the resultant device structure was extremely rugged and fault tolerant, allowing sufficient time to sense the fault and safely switch off the device without thermal damage.

1.4 Thesis overview

Firstly, a thorough review will be completed in chapter 2 of the targeted application within aircraft and the state of the art solid state switching devices available towards meeting those requirements. The alternative state of the art materials and device structures will also be compared and contrasted to determine the best direction of the novel hybrid design and development stage of the research. The optimisation of a standard unipolar Vertical Double diffused MOSFET (VDMOSFET) in silicon for lowest possible static loss will be described in chapter 3 which utilised a statistically based, structured Design Of Experiment (DOE) approach. The optimised VDMOSFET would form the basis of the hybrid unipolar-bipolar device. Various methods will then be described in chapter 4 as to how to achieve a state of conductivity modulation, within the hybrid, resulting in a reduced resistance and hence

lower static loss in the ‘on’ or conducting state when compared to the standard MOSFET. The means of also obtaining bipolar conduction within the conductivity modulated hybrid will then be demonstrated through incorporation of both an emitter and separate collection centre for the hole carriers operating in parallel with the unipolar (electron) conduction path. The emitter structure utilised was similar to that used within a Junction Barrier Schottky (JBS) diode, Baliga[9] to form a merged Schottky/acceptor doped anode which could be placed either vertically or laterally relative to the MOS channel region.

The operation and forward biasing of the emitter relative to the N-Drift region will then be described in chapter 5 as regards to the vertical and lateral emitter position relative to the channel. A static performance comparison of the emitter structure as placed either vertically or laterally using the same MOS channel structure and semiconductor thickness will then be completed and any compromises discussed within chapter 6. The method of optimising the vertical and lateral hybrid devices will also be examined in chapter 6 in order to select which was the best structure to meet the design aims of the research and hence which structure would go forward into the assessment phase of the dynamic loss performance within chapter 7. The lateral hybrid device structure will be compared directly to a standard unipolar VDMOSFET and bipolar Non Punch Through IGBT of the identical BV rating to assess the performance over changes in ambient heat sink temperature (T). Any benefit of the hybrid, relative to the mainstream device types, will then be assessed using standard figures of merit such as specific on state resistance $R_{(ON,SP)}$, active device area (A) and turn off energy loss (E_{off}). In particular the susceptibility to ‘latch-up’ will be assessed, which is a condition affecting only bipolar devices where all gate control is lost due to high hole current flow. Finally, in chapter 8 conclusions will be drawn as to the benefits of the new hybrid design concept relative to the VDMOSFET and non punch through IGBT types. In the recommendations section of chapter 8 a revised device structure will be presented to boost the rating voltage of the concept from 100 V to above the minimum application requirement of $BV=500$ V whilst simultaneously improving the bipolar current conduction

performance by minimisation of the base width (B_w) of the bipolar conduction device. In addition recommendations for further study include the need for 3D simulations to assess the affect of varying the P-Anode and Schottky area relative to the MOS channel area, and the effect of varying the metal work function used for the Schottky contact. Further applications of the resulting low loss, latch up free, fast switching lateral device type are also suggested.

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Chapter 2 | Motivation and background

2.0 Introduction

Within this chapter the motivation for the research work will be described as related to the More Electric Aircraft (MEA). Firstly, the reasons why the MEA is a globally significant design goal will be explained. As a direct consequence of that design goal then the impact of increasing the electrical load on the electrical power distribution system within the MEA will be described. The limitations of the existing power distribution switching technology will then be reviewed and a specification for the required switching element will be created. A review of the state of the art power semiconductor switching technology as relevant to the resultant switch specification will be completed in order to ascertain a direction for the research work.

2.1 Motivations

The aims of the More Electric Aircraft (MEA) design will be reviewed in this section and the consequences of those requirements on the electrical power distribution will be highlighted. Those requirements will then be used to develop a specification for the primary node switching element to be used within the MEA.

2.1.1 Application description

The need for the MEA arose directly from the global need to minimise carbon dioxide (CO₂) released during the combustion cycle of carbon based fuels. The Kyoto agreement of 1997 was the first treaty between countries to minimise global emissions of CO₂. The direct effect

of the treaty on Europe alone was to reduce the collective emissions of CO₂ to 8 % below the 1990 levels by 2012 according to the European commission for climate action[1], this was further extended in 2007 to commit to a 20 % reduction by 2020. The agreement made in Cancún during 2010 marked an important step to making a comprehensive and legally binding framework to legislate beyond 2012, the end date of the Kyoto agreement. A report edited by Krzyzanowski[2] on behalf of the World Health Organization (WHO) explained the effects on health of transport related air pollution which reinforced the need to reduce the use of carbon based combustion fuels. In the United Kingdom the government [3] have stated that in 2012 approximately 6.4% of the main greenhouse gas (CO₂) emissions from the U.K was directly contributed by aircraft and by 2020 this was expected to be 10 % due to the increased demand for air travel.

The MEA, like all aircraft, would combust carbon fuels for propulsion. In previous aircraft, developed adhoc over decades, the energy from the combustion was also converted in to four other forms: pneumatic, hydraulic, mechanical and electrical energy as described by Rosero[4]. The aims of the MEA were to gain fuel efficiencies through removal of all conversions other than that of converting to electrical energy via the use of generators. Indeed, the MEA program run by the U.S. Air Force aimed to deliver a Power Optimized Aircraft (POA) which reduced non propulsion power, to improve fuel efficiency, while increasing the reliability and safety of on board systems and reducing maintenance costs, again as described by Rosero[4]. The targeted reliability improvements of MEAs as compared to conventional aircraft technology were between 1400 to 1900 % while offering a 200 % improvement in power density as discussed by Cloyd[5].

The changes necessary to the power distribution system for the MEA meant that increased power distribution voltages would be required in order to limit conduction losses, reduce cable size and hence weight, as described by Avery[6]. The targeted distribution voltage was +/- 270 V dc (load voltage =540 V) as described by Avery. In the event of generator failure the Auxiliary Power Unit (APU) would supply power again at +/- 270 V

dc. It is likely that some form of energy storage would be used as the APU, one example being the hybrid fuel cell and Li-ion batteries as described by Eid[7]. Such Li-ion batteries have high energy storage and can reach extremely high short circuit currents (measured at a peak of 11,697 A with the full cell capacity being delivered within a three minute duration using a 50 Ah battery) as described by Issacs[8].

The power management and distribution system development for an MEA project in the U.S. was described by Maldonado[9]. Maldonado described that the power distribution system was required to not only minimise weight and maximise supply power availability, but also to maximise reliability and therefore have high fault tolerance. The power switching element was the most essential part of the power distribution network. The essential purpose of the switch was to protect the hundreds of kilometres of insulated wire in order to prevent loss of power, loss of loads and reduce fire hazard as described by Bailey[10]. The critical nature of the aircraft application meant that safety and reliability was the key factor, as described by Bailey[10], such that:

- a) No single failure shall lead to a loss of power channel
- b) Fail safe switch node mechanisms were required
- c) No cascading failures allowed
- d) No common mode failures allowed
- e) Must be designed for 24 year service life
- f) Must operate reliably in harsh environments: EMC, vibration, acoustic noise

Each switching node, called an Electrical Load Management Centre (ELMC) by Maldonado, consisted of a Solid State Power Controller (SSPC) and a microprocessor controlled fault detection system which provided a programmable overload curve (I^2t) and current limiting, plus a fast acting short circuit trip (10 μ s), again as described by Maldonado[9]. Thus, any switching element used in the SSPC had to withstand fault current conduction for a minimum of 10 μ s.

The SSPC shown in figure 2.1 was described by Friedman[11] and utilised solid state switching devices instead of older Contact Breaker (CB) technology. The



Figure 2.1. Two examples of solid state SSPC units as supplied by Data Device Corporation [11, 12].

specifications or CB technology, such as the EV200 series, as manufactured by Tyco Electronics Corp[13], demonstrated the main problem concerning reliability of the CB, or electro-mechanical contactor. The CB was guaranteed to break only above 650 A, and also required replacement in the event of breaking a high magnitude fault current of >2000 A (at 270 V) as shown in figure 2.2. It was also possible for the contacts to weld shut due to arcing if the current exceeded that specified by the manufacturer, for example if Li-ion batteries were used then short circuit current could be >5 times larger than the Tyco maximum break current specification as described by Issacs[8]. However, CBs were still the preferred solution at nominal currents of 50 A to 500 A as described by Bailey[10] when speaking in 2009 due to the very low on state resistance (where on state resistance, $R_{ON} = 0.2$ m Ω in the EV200 series). In addition CBs had a high power density and were proven to be robust to high temperature operation and voltage transients; they also offered good isolation as provided by the air gap within the CB. Unfortunately, CBs were slow to switch, they required additional electronics to provide protection from high current, and they offered no means to control the current magnitude, again as described by Bailey[10].

Another important reason for requiring solid state replacement of CB technology was provided by Friedman[11] and Simon[14] in that computer control of the power distribution system enabled remote placement of the ELMC between generator and loads directly, instead of routing heavy cabling via the flight engineers fuse panel. Status of the EMLC could then be relayed back to the control computer in real time due to the speed

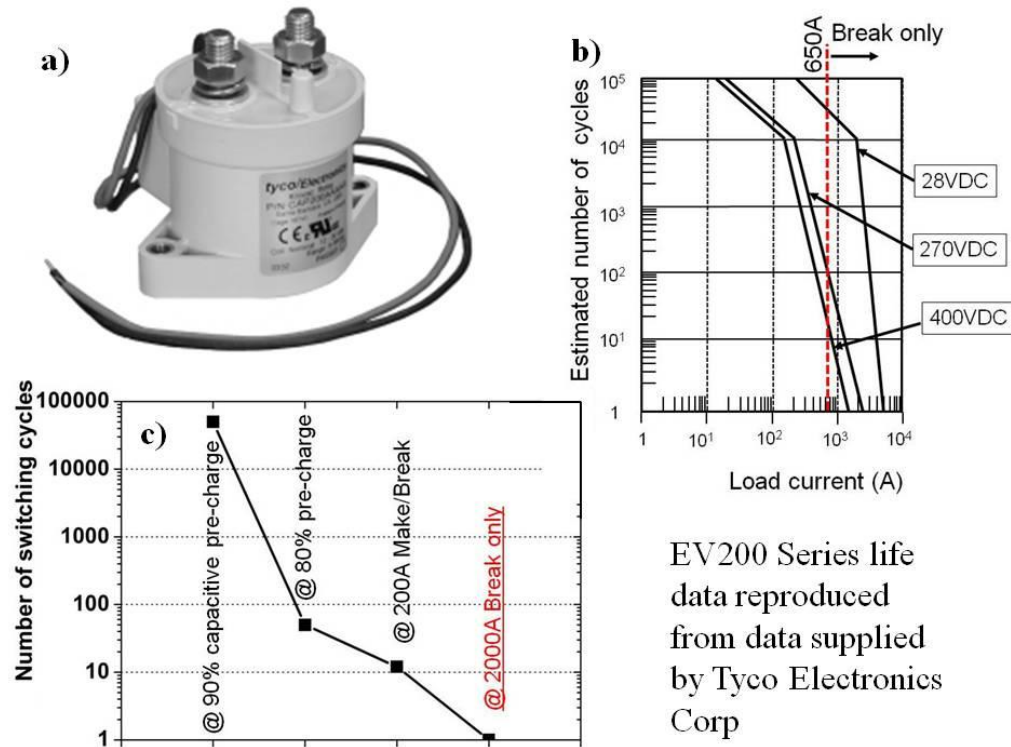


Figure 2.2. a) A typical electro-mechanical contactor; b) and c) associated switching cycle life data reproduced from manufacturers data.

of the solid state devices. Bailey[15] agreed that the main advantage of the solid state ELMCs was that they could be positioned in remote locations directly between the bus and the load to form an overall distribution network, the optimisation of which could be tailored to each aircraft. Indeed Bailey went on to say that the SSPC solution offered a means to the provision of enhanced diagnosis and prognosis of problems. Such SSPC enabled distribution networks at +/- 270 V dc could be modelled, as demonstrated by Izquierdo[16]. The work of Izquierdo demonstrated the ability of the software tools to optimise and verify any layout, thus highlighting any potential issues through both secondary and primary switch nodes in the event of changing a load or SSPC type for example.

The solid state switching devices were beneficial in a computer controlled system due to the greatly reduced the switching time ($t_{off} = 12$ ms in the case of the EV200 series), which eliminated contact bounce as described by Barrado[17], thus providing a reliable high fault current turn off capability. The solid state device solution to the needs of a remote ELMC however, raised a few new problems. As described by Simon[14] the solid state devices available to an SSPC designer could never match the low on state resistance of the contact breaker (CB). Due to the requirement for the use of solid state devices with a minimum $BV > 500$ V (from MIL-STD-704-F[18]) then increased junction temperature within the semiconductor, relative to a lower BV device, were anticipated but, according to Simon[14] the airframe had no capability to remove heat generated from excess power dissipation easily, power dissipation therefore needed to be minimised to reduce self heating. Unlike the CB solution, according to Simon[14] and Bailey[10], the SSPC could not provide galvanic isolation therefore leakage levels from the solid state power devices was required to be very low (<1 mA), even at high temperatures.

Finally, the electrical loading supplied via an SSPC would predominately be inductive in nature as described by Weimer[19]. The switching device therefore would need to achieve low static conduction losses, a high current switching capability and demonstrate lowest dynamic losses during that switching event to prevent device failure for reasons of transient lattice heating.

2.1.2 Target specification for the SSPC switching element

The key requirements of the switching element are summarised in table 2.1 for the proof of the injection concept device. Each requirement is ranked in terms of priority. The concept was to be proven at low voltage then a device structure found to boost the BV and hence supply voltage to that required by MIL-STD-704-F[18]. The basic schematic of the presently used power controller incorporating CB's for the power switching elements is shown in figure 2.3 demonstrating

Factor	Requirement	Reason
1	$BV \approx 100$ V minimum	Injection concept proof only
2	Operational temperature	-40 to +85 °C (233 to 358 K), higher preferred
3	High fault current tolerance	Use of Li-ion batteries
4	High reliability	Remote location, restricted access, minimise
5	Voltage control	Remote location, restricted access, minimise wiring weight, saves fuel
6	Lowest static conduction loss	More of the generated power gets to aircraft systems, saves fuel. No heat dissipation capability in airframe
7	Lowest dynamic loss	Prevent thermal failure during fault switching transient (in 500 V device)
8	Low leakage current	Loss of galvanic isolation through removal of CB

Table 2.1. Summary of targeted switching element characteristics within an SSPC.

how 540 V is obtained across the load from a ± 270 V dc supply. The aims of this research project was to identify the lowest loss semiconductor switching elements to replace the single pole single throw CBs as shown in figure 2.3.

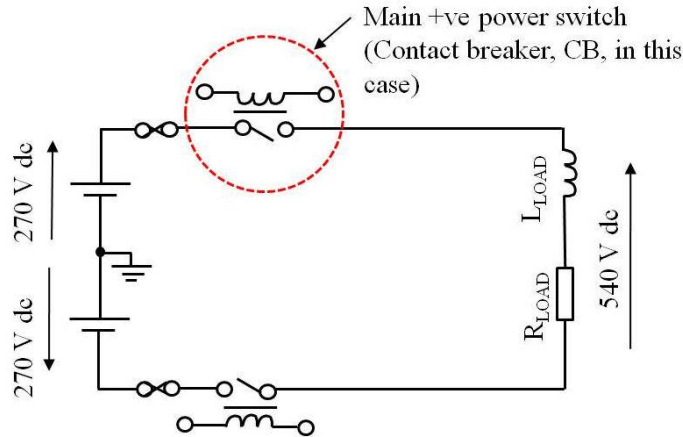


Figure 2.3. Power switching element of an EMLC using contact breakers.

2.2 Background

Having established the motivation for the work, this section forms a review of the SSPC developments to Oct 2008 when the research project started and assesses the choice of power semiconductor switching element in terms of the summary of requirements shown in table 2.1. Since 2008 significant improvements in wide band semiconductor research has been demonstrated, but what is shown herein set the course and direction of the research. The recent developments in the identified key semiconductor device technologies will then

be assessed to establish the potential performance benefits to the SSPC. In addition SSPC developments since Oct 2008 will also be used to demonstrate the issues with some of the new wide band gap device technologies.

2.2.1 Solid state devices used in SSPC development

The limitations of solid state devices as regards application to SSPC development was summarised by Bailey[10]. He believed that the following limitations existed:-

- 1) High operating temperature limited to 100 °C.
- 2) Voltage transients could cause damage
- 3) The switching of capacitive and inductive loads was required
- 4) Solid state devices produced excessive heat due to a much higher voltage drop
- 5) The safe operating area was restricting
- 6) The ability to current share equally when multi-die construction was used was a key concern to prevent cascade failure

Although written in general terms, the above applied to silicon Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). As confirmed by Friedman[12] who described that the MOSFET solution enabled a parallel die solution, whose current share was equalised due to the positive temperature coefficient of the MOSFET, as confirmed by Ahmed[20], but was susceptible to voltage transients when switching off inductive loads. The work of Friedman[12] also included some “bipolar monolithic” devices which operated in parallel to the MOSFETs. As explained by Barrado[17] developed SSPC units commonly used silicon MOSFET or Insulated Gate Bipolar Transistor (IGBT) devices as power switching elements, these were also compared by Liu[21]. Liu came to the conclusion that the bipolar IGBT offered the lowest loss solution and a means of reducing the active area of MOSFETs as he stated that a quantity of 30 “CoolMOS” MOSFETs from Infineon[22] were required to replace a single IGBT. Liu confirmed also that the IGBT also enabled significant reduction in on state voltage drop at a given current level. Ahmed[20] however, chose to use the “CoolMOS” MOSFET type arguing that bipolar devices types all demonstrated a P-N

junction forward volt drop = built in potential of the junction (V_{BI}) and therefore they have a fixed voltage drop prior to any conduction, whereas MOSFET devices did not and hence were most suitable for conducting with a forward volt drop in the range of 0.1 V to 0.8 V. Ahmed[20] also stated that the MOSFET had very fast rise and fall time during switching, short storage times, excellent safe operating area and simple drive requirements. The CoolMOS MOSFET type enabled reduction of the on state loss through reduction of the N-Drift thickness and increased n-type doping made possible by charge balance techniques, as first described by Deboy[23] in 1998 and later by Lorenz[24].

All the above devices were fabricated using silicon which according to Liu[21] had a maximum operating temperature of 150 °C as confirmed by Infineon[22]. Whereas the use of devices fabricated from wide band gap materials offered the opportunity to increase the operating temperature while also offering a theoretical reduction in on state voltage drop. For example Feng[25] demonstrated an SSPC utilising a silicon carbide (SiC) JFET as the switching element. Although a low static loss was achieved wherein the SSPC design, capable of conducting 30 A continuously, conducted fault current at 1000 % the continuous rating (300 A) for 10 ms, using 0.34 cm² of JFET SiC area as compared to 9 cm² of silicon MOSFET area to conduct the same current over the same time period. Unfortunately, due to the SiC JFET being a normally on device the 28 V dc supply was required to be permanently on to ensure that the JFET device controlling the 270 V bus could be turned off. The inherent safety of the SiC JFET SSPC was therefore questionable as normally off devices are generally considered as electrically safe in the event of load circuit maintenance. The JFET, however has the potential to provide one of the lowest $R_{(ON,SP)}$ device types and could provide a normally off operation via the ‘Cascode’ configuration. The resulting normally off, low $R_{(ON,SP)}$ switch therefore did not suffer from MOS channel related mobility issues as per the SiC MOSFET. The upper temperature limit of the Cascode configured solution unfortunately would be limited to around 150 °C, in the case where a silicon MOSFET is used to drive the SiC JFET. Thus one of the positive impacts of using a high operating temperature SiC device is therefore reduced. Much of the upper operating temperature

capability however, depends strongly on the device packaging and attainment of the lowest thermal impedance possible junction to infinite heat sink.

A silicon carbide (SiC) MOSFET was also trialled within an SSPC as demonstrated by Guo[26] . In theory a lower on state resistance was possible in SiC than in Silicon due to much reduced N-Drift thickness made possible by a ten times higher critical electric field (ϵ_{crit}) than silicon thus enabling a higher N-Drift donor doping. Guo[26] found that sixteen of the SiC die were required to conduct the required current due to the low mobility in the SiC MOSFET channel which meant that a higher specific on state resistance, $R_{(ON,SP)}$ for a given blocking voltage (BV) was obtained than theory predicted, hence more die were required.

2.3 Solid state devices device type comparison

A thorough review of available solid state switching device types was required to ensure that all potential device types were considered. This review included the use of silicon, two types of device will be considered: bipolar and unipolar devices. In section 2.4 wide band gap materials will be considered.

2.3.1 Bipolar voltage controlled devices

Bipolar switching semiconductor device classes such as the Bipolar Junction Transistor (BJT), thyristors and Gate Turn Off thyristors (GTOs) were ignored by the developers of the SSPCs as investigated in the preceding section. This was due to the high current drive required to gate them and hence the weight and complexity of the driver circuits. The thyristor type however, due to the bipolar conduction state offered the lowest on state resistance for the largest blocking voltage (BV), such types therefore are used in applications requiring a BV of > 6 kV, such as HVDC links as discussed by Baliga[27]. The Thyristor demonstrates a forward volt drop (V_{AK}) ≈ 1 to 2 V which is relatively small at $BV = 6$ kV, but not at $BV = 500$ V, which was required in this application.

Instead of the current control, as required for the above range of bipolar devices, the SSPC developers favoured the use of voltage control, to enable the use of lighter weight cables and control of the remote SSPC. Voltage control was available through the use of a

Metal Oxide Semiconductor (MOS) gate, only a very small current was required to charge the total MOS capacitance. Two key classes of semiconductor device technologies, that were both bipolar and MOS gate controlled, these were the Insulated Gate Bipolar Transistor (IGBT) and the MOS Controlled Thyristor (MCT). Many types of MCT were developed in the period between 1989 and 1998 as shown in literature, but no current manufacturers could be located of this class of MOS gated device due to the dominance of IGBT technology. In addition the MCT had an issue with the relatively low level of maximum controllable current in comparison to the IGBT. Though the possibility of achieving a high current MOS gate controlled MCT has led to much work for example by Flores[28]. An example of an N channel MCT and the P channel MCT, both with N-Drift regions, were described by Huang[29] and Bauer[30] respectively are shown in figure 2.4. The MCT

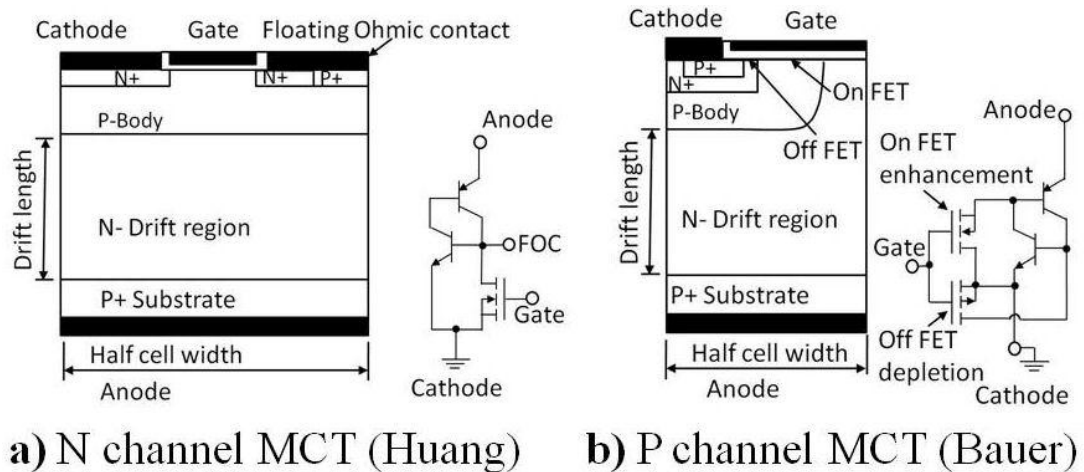


Figure 2.4. Comparison of MCT Thyristor structures: a) N channel and b) P channel turn off devices.

structure reviewed by Trivedi[31] utilised a P-Drift region as compared to an IGBT with an N-Drift region. These types were directly compared by Trivedi[31] in terms of their switching capability. The key conclusion was that the dynamic losses of the MCT were much higher than the IGBT. Due to the increased charge storage level, however the on state resistance of the MCT was lower. Trivedi[31] stated that the turn off loss was so large in the MCT that it negated any benefit of the reduced on state loss. A comparison of an MCT as per the structure used by Bauer[30], an IGBT (as per Trivedi[31]) and the Emitter Switched

Thyristor (EST) was completed by Tan[32]. Each structure was designed to have a BV of 600 V using the identical P-body and P-Anode acceptor doping. The MCT clearly demonstrated lowest on state loss and highest saturation current level followed by the IGBT and then EST. Unfortunately, the MCT was stated not to provide a realistic turn-off capability, thus only the EST and IGBT were compared. Of those the IGBT was concluded to be a marginal improvement as both device displayed long tail current due to hole storage requiring recombination. The MCT, for reasons of poor turn-off characteristic, and the EST, for reasons of low saturation current, were concluded to be unsuitable for the SSPC.

2.3.2 Comparison of MOS gated unipolar and bipolar devices

The MOS gated bipolar IGBT was the choice of Liu[21] for the SSPC design, whereas the unipolar MOSFET was the choice of Ahmed[20]. Friedman[12] and Komatsu[33] also chose the MOSFET for use in a power distribution switch intended for space applications. As shown in figure 2.5 the MOSFET and the Non Punch Through (NPT) IGBT have very similar structures in terms of the MOS gate and cathode connection. The anode however, is N^+ doped for the unipolar MOSFET and P^+ doped for the IGBT. The drift length of the N-drift region between the MOS P-body and the substrate in both structures is fixed by the maximum depletion extent from the reverse biased P-body to N-Drift junction at the specified BV . The doping of the N-Drift region (and P-body to a lesser extent) sets the 1-Dimensional (1-D), or doping dependant BV to the limit imposed by the critical electric field (\mathcal{E}_{CRIT}) which for silicon is in the region of $2-3 \times 10^5$ V/cm. Due to the larger BV rating generally required of the IGBT when compared to a MOSFET then the N-Drift region doping is lower than that of the MOSFET. The Drift length of the IGBT is also thicker and for that reason the NPT IGBT is fabricated on bulk (float zone) wafers with an implanted (shallow) P-Anode into the reverse side of the wafer (the MOS gate side being the top of the wafer). The NPT device has no epitaxial layer growth and the float zone wafers may also be thinned dependent upon the required BV rating. The epitaxial layer grown on to an N type substrate is however, required in a MOSFET to ensure even resistivity (ρ), in units of Ωcm ,

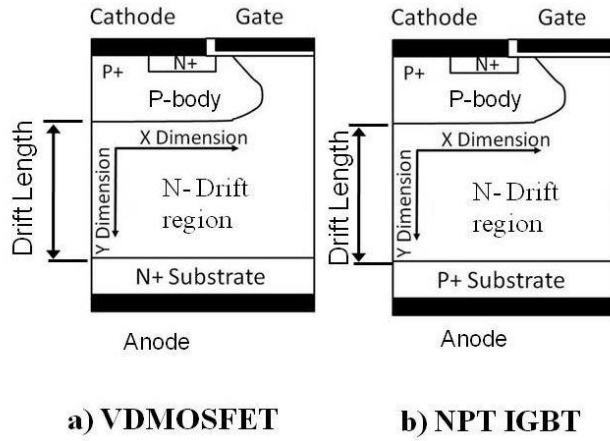


Figure 2.5. Comparison of a) the unipolar MOSFET structure and b) the bipolar Non Punch Through (NPT) IGBT structure both using a DMOS type gate design.

throughout the entire volume of the layer to indicate an even distribution of donor doping, usually Antimony (Sb), in order to achieve low on state resistance. The Punch Through (PT) IGBT however, is more similar in construction to the MOSFET as it too uses an n-type epitaxial layer growth, but on this occasion on to a p-type substrate (for an higher mobility, lower loss ‘N channel’ device).

The development of MOSFETs and IGBT class devices have always been closely linked for the above reasons, developments to boost the MOSFET performance have therefore shortly afterward been used in the IGBT such as changes to the design and fabrication of the MOS channel. The use of charge balance techniques is another example. Some developments such as the use of field stop technology and life killing irradiation techniques have been made purely for the IGBT, to improve the Punch Through (PT) or asymmetrical IGBT performance and required silicon area. There follows a description of the technical advances in IGBT technology.

2.3.3 Original DMOS bipolar IGBT devices

DMOS (Double diffused Metal Oxide Semiconductor) technology, describing how the cathode, gate region and P-body is formed, enabled the first commercially available IGBT type, originally called a COMFET in 1984, Russell[34]. This first device type became known as the Non Punch-through (NPT) DMOS or ‘Planar’ IGBT. Baliga[35] was the first

to use the description “Insulated Gate Bipolar Transistor”. A direct comparison of the structures for an NPT and a PT IGBT are shown in figure 2.6. In 1996 Baliga[36] wrote a summary of the trends in power semiconductor devices to that date. In this document the NPT IGBT device performance, in terms of the compromise between on state voltage drop and turn-off time, was improved by use of the Punch-through structure (PT). Further stating that PT structures were suitable up to forward blocking voltages of 1200 V, whereas NPT structures were suitable for devices of >1500 V withstand. The reasons for this was described by Lorenz[37] where as the PT structure was fabricated within epitaxial material,

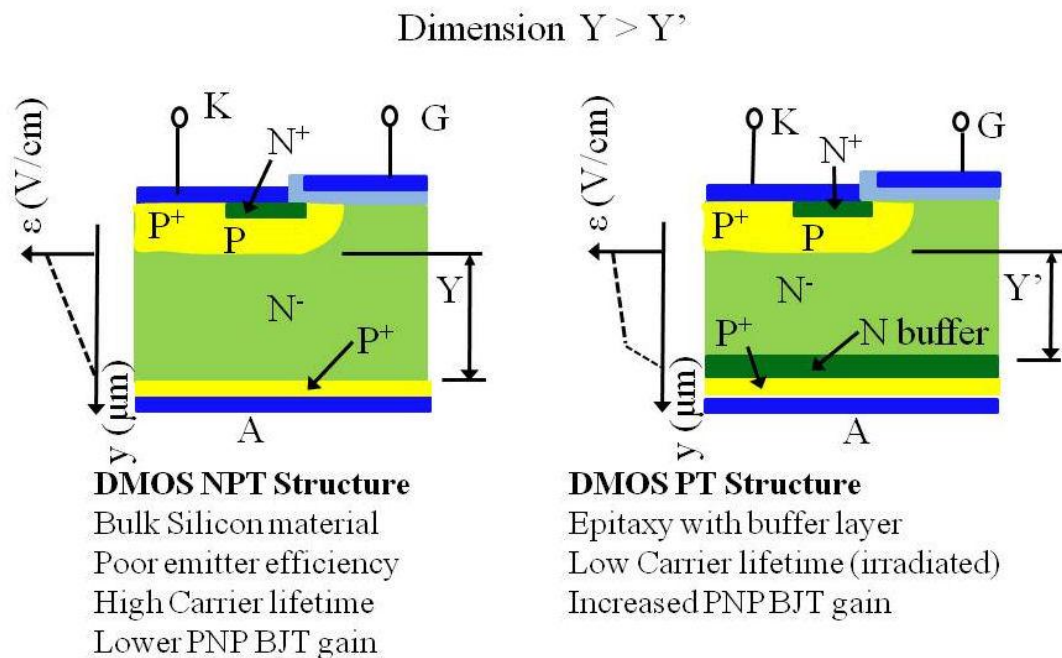


Figure 2.6. Comparison of DMOS NPT IGBT and a DMOS PT IGBT type (incorporating a field stop, or N buffer layer).

the cost of epitaxial growth effectively capped the maximum voltage withstand available. Due to the PT device being fabricated within an epitaxial layer it was characterized by high P-Anode (emitter) efficiency which had the benefit of reduced on state voltage drop, fast turn on times and therefore reduced losses. However, lifetime control was required in a PT device to encourage faster recombination, and therefore speed up turn off times and reduce dynamic losses at turn off.

Due to increased emitter efficiency of the PT structure and hence increased hole concentration in the N-Drift region irradiation was required to reduce the lifetime of the stored charge in the N-Drift region according to Deboy[38]. The technique, although successful in reducing turn off times, was found to lead to an increased on state voltage drop (V_{AK}) within an NPT IGBT as described by Baliga[39]. However, Mori[40] found the turn off time and therefore turn off losses were reduced by roughly a half using this technique in a PT IGBT, even at high operating temperatures of (125 °C). The effect on forward voltage drop of the irradiated PT device was not directly made in the paper by Mori[40], Deboy[38] however stated that the PT device provided the lowest on state voltage when compared to an NPT due to the reduced PNP BJT base width (B_W) (where dimension $Y' < Y$ in figure 2.6). Comparison was drawn by Mori[40], between uniform lifetime PT devices and some of the same structure with local lifetime control, wherein the on state voltage drop (in terms of the anode to cathode voltage, V_{AK}) appeared not to change in those subject to local lifetime control. PT devices, as a result, therefore benefit from an improved V_{AK} / t_{off} performance compromise over and above NPT devices.

The NPT devices emitter efficiency could also be adjusted by ion implantation dose and annealing according to Lorenz[37] again in order to reduce the on state voltage and improve turn on times if necessary to the application, but not achieve the same benefit as the PT type. The NPT device however was also known as a reverse blocking IGBT structure, or symmetrical voltage blocking device, Motto[41], in that the reverse and forward blocking voltage are identical. This had advantages in alternating current (ac) control switch applications as the series diodes necessary for reverse blocking when using PT IGBT devices could be removed reducing the overall forward voltage drop. PT IGBT devices had a lower reverse blocking capability (BV_R) than NPT devices due to the thinner drift region and use of the buffer layer according to Mohan[42]. The buffer layer was known as a field stop layer which enabled minimisation of the N-Drift region length and hence reduced PNP BJT base width (B_W) as described by Deboy[38].

Of particular importance for paralleled devices, the NPT IGBT type had a positive temperature coefficient in terms of increasing on state resistance with rising temperature. Whereas at low currents the PT device has a negative temperature coefficient which reverted to a positive coefficient above a certain current threshold point according to Bontemps[43]. PT type IGBTs therefore required careful operating point design as negative temperature coefficients led to instability when die were operated in parallel. MOSFETs were stated to have a positive temperature coefficient according to Bontemps.

2.3.4 Development of the IGBT type of bipolar devices

According to the work of Udrea[44], both DMOS type of devices (PT and NPT) previously suffered from the phenomenon called ‘latch up’ wherein a parasitic thyristor latches on and thus gate control of the device conduction was lost, potentially leading to thermal runaway and device failure. This phenomenon could be caused by over voltage (static latch up), or dynamically due to switching off an inductive load, the cause was the resulting high current of holes via the P-body which developed sufficient voltage drop to forward bias the emitter-base junction of the parasitic NPN type BJT. An improved MOS gate design however, was called the Trench (or UMOS). The Trench gate design enabled higher packing densities in both MOSFET and IGBT designs which translated in to a lower area specific on state resistance $R_{(ON,SP)}$ in MOSFET designs as an increased channel area to cell width ratio was achieved. A typical trench gate design in comparison to a DMOS gate is shown in figure 2.7, where the dimensions X and X’ indicates the relative half cell width achieved in the DMOS and trench structures, respectively.

Although still affected by latch up the Trench, or UMOS, structure provided a factor of four times improvement in static latch up immunity and a factor of two times improvement in the magnitude of controllable current switch off into an inductive load according to Udrea[44]. Harada [45] supported the work of Udrea[44]. Harada stated that the latch up immunity of the UMOS device was better than DMOS after producing and testing a $BV=600\text{ V}$, $I_K=50\text{ A}$, UMOS device type. However, the work of Trivedi[46] used simulated

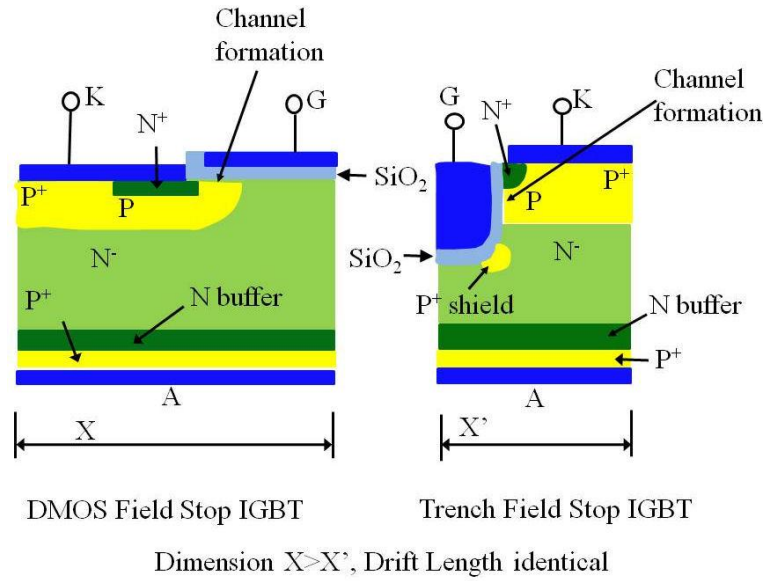


Figure 2.7. Comparison of DMOS and trench Field Stop IGBT (both PT designs).

structures, as a result he stated that due to the higher current densities within the UMOS structure then this device type was more susceptible to latch up than DMOS. The problems of latch up have since been overcome in both DMOS and UMOS designs through incorporation of a deeper P+ region and reduced N+ cathode length as described by Baliga[27].

Udrea[44] explained that DMOS types also suffered from a parasitic JFET effect, which is to the detriment of the on state resistance at high V_{AK} due to the electron current being restrained by a depletion region formed between the p-bodies of two adjacent half cells, into the wide N-Drift region. Udrea[44] confirmed that the JFET effect was removed within the Trench or UMOS structure due to the deep vertical gate channel. In addition, the trade off between the bipolar start up voltage (V_i) in terms of V_{AK} and turn off times within the UMOS design was explained by Udrea[47] to be much improved over DMOS devices. The work of Mori[48] and Harada[45] confirmed the lower on state voltage drop of the UMOS device type relative to the DMOS type. The other advantage of a UMOS device was that it provided a lower on state resistance to when compared to the state of the art DMOS technologies according to work again completed by Udrea[47]. Indeed, the trench gate feature was described by Harada[45] to make the UMOS IGBT device perform more like a

MOS gate and PiN Diode, thus creating a more ideal voltage controlled, low on state resistance device. Again, irradiation was utilized by Harada[45] to improve switching performance which resulted in reduction of turn off losses, but at the cost of increasing the on state voltage (in terms of V_{AK}). Without irradiation Udrea[47] fabricated a 1.2 kV capable device which had an on state voltage drop of 1.1V at 125°C, this according to Udrea equated to a lower on state resistance than DMOS types. Again, this finding was supported by the work of Harada[45]. In addition Harada found that UMOS devices also supported a higher breakdown voltage than DMOS.

2.3.5 Compared reliability of the IGBT type of bipolar devices

Ignoring latch up due to the design improvements described by Baliga[27], a summary of IGBT short circuit failure modes (applicable to DMOS and UMOS) was provided by Lefebvre[49] as follows:-

- 1) Power limited failure- as described by Laska[50] & Otsuki[51] essentially failure occurred at or near the peak current at the beginning of a short circuit.
- 2) Energy limited failure- as described by Trivedi[52] essentially the IGBT failed during the short circuit due to overheating the silicon lattice which led to thermal runaway.
- 3) Delayed failure mode- as described by Laska[50], Gutsman[53] and Otsuki[51] essentially where failure occurred several hundred μ s after the IGBT had switched off the short circuit due to over voltage as caused by the voltage generated in an inductive load or due to stray inductance in the circuit or power module as described by Chokhawala[54, 55].
- 4) Inhomogeneous operation failure, as described by Yamashita[56], essentially where one part of the gate electrode had a lower MOS threshold voltage (V_{TH}) than another (perhaps due to manufacture or uneven temperature distribution) leading to unbalanced current distribution and hot spot formation. Failure looked like dynamic latch up as described by Laska[50] and Saint-Eve[57].

Importantly, to the SSPC design, the work of Laska[58] described the superior short circuit ruggedness of NPT devices over PT devices. The benefits, according to Laska[58], stemmed from the NPT operation, wherein the device was governed by a field dominated current (drift current) even under short circuit conditions, whereas the PT device operated with a current flow dominated by the diffusion mechanism. The injection efficiency of the PT type was also improved over the NPT type according to Laska[58]. In addition the PT IGBT had reduced drift length, thus the integral PNP BJT within the PT IGBT had improved current gain. The higher the current gain, the higher the short circuit current, and the lower the short circuit withstand time, as described by Chokhawala[54]. As a result of these effects within the NPT IGBT there was a flat current density response and voltage characteristic over time following the application of a short circuit across the load at saturation, whereas for the PT device the current kept increasing over the same duration of time until thermal failure. Laska[58] went on to state that there remained however, a compromise which existed between turn off time, resulting in ‘tail’ current (hence turn off losses) and on state voltage drop as the PT device essentially switched faster than the NPT device.

Failure within the DMOS PT IGBT structure due to short circuit was analysed by Trivedi[52] via the use of simulation techniques. Within the PT structure the hottest part of the lattice was located directly under the gate electrode near the channel due to the high current density of the short circuit current, this gave rise to multiplication of thermally generated carriers which eventually caused failure. Failure was not caused by latch-up as was the widely held assumption at the time (1998).

In terms of the endurance time for short circuit conditions of $V_{AK} = 600$ V, gate voltage (V_{GK}) = 15 V then the UMOS or trench device created by Udrea[47] was 12 μ S with a maximum controllable current density of 1000 A/cm². This trench type of device however, according to Mori[48] was not as rugged against short circuit failure as the original DMOS type and was in agreement with Chokhawala[54]. This was due to the high saturation collector (anode) current density, $J_{A,sat}$ of the trench type of device as opposed to the larger

cell width of the DMOS. An improvement to the Trench design was proposed by Mori[48] which used a High conductivity IGBT (HiGT) structure, this HiGT structure which utilised a trench gate was discussed as also having lower on state voltage drop when compared to DMOS, but also an improved on state resistance and better short circuit capability when compared to the standard UMOS. Unfortunately, this work was only at current densities of $J_{A,sat} = 200 \text{ A/cm}^2$ which is not directly comparable to other works. The high saturation current density of a UMOS type was confirmed by Udrea[44] as $J_{A,sat} = 2000 \text{ A/cm}^2$. Short circuit failure of the device fabricated by Udrea was therefore stated to be by direct thermal effects. The work of Benmansour[59], Otsuki[51] and Trivedi[46] supported the finding that UMOS could not support short circuit current for as long as an DMOS IGBT type. Although the UMOS Field Stop PT IGBT, such as the IGP30N60T from Infineon[60], appeared to have a better t_{off} / on state voltage drop trade off, an improved latch up resilience, and removal of the JFET effect, it does still however, have reported results showing lower short circuit ruggedness when compared to NPT DMOS IGBT. It also has the added potential for oxide breakdown problems. In the case of the work of Trivedi[46] for example he determined through simulation that the NPT UMOS device as modelled had failed under short circuit condition within 1 μs due to a ‘hot spot’ formation below the trench feature. He stated that this was due to the high electric field leading to thermally assisted carrier multiplication. The NPT DMOS device however, as modelled by Trivedi[46], failed under the same short circuit conditions in 15 μs . Baliga[36] however, believed that the Safe operating area (SOA) of the UMOS type had been shown to be superior to that of the DMOS type and expected UMOS to replace DMOS in most applications up to 1.2 kV as a result. Udrea[44] however, stated that the short circuit endurance time of the UMOS device type was less than that of DMOS, however UMOS offered a better trade off between on state loss and short circuit performance. The short circuit endurance of UMOS compared against DMOS was also confirmed by Mori[48] stating that the reason for early short circuit failure of UMOS was high saturation collector (anode) current density $J_{A,sat}$. Trivedi[46] stated that UMOS should be used with external short circuit protection circuitry as a result of its

reduced ruggedness, however DMOS NPT devices could be used without external protection. Chokhawala[54] supported the work of Trivedi stating that due to the higher gain of the PT UMOS device, then greater external circuitry protection against short circuit was required as compared to the lower gain NPT-IGBT type. If required, then in both PT and NPT device types the anode-cathode voltage (V_{AK}) could be used to monitor for short circuit current for external short circuit control as described by Eckel[61].

Additional problems have been reported with the UMOS device type, such as difficulties with manufacture, these are as regards the requirement for deep trenches necessary for higher blocking voltage devices, hence device availability to 1.2 kV only according to Baliga[36] in 1996. According to Udrea[47], writing in 1999, devices at that time were prone to premature breakdown problems and degradation of inversion layer mobility (μ_{ni}). The premature breakdown problem with UMOS was described by Lee[62] in that high electric fields were generated at the gate oxide interface at the corners of the trench and thus the trench gate oxide may breakdown at those points. The solution described by Lee[62] was to demonstrate that a P+ type implant (forming a shielding layer) placed at the trench corners reduced the electric fields formed there as shown in figure 2.7.

In the SSPC application there was no requirement for fast switching (other than to reduce dynamic losses) therefore the benefit of UMOS was not apparent in terms of the high priority placed on reliability as shown in table 2.1. The added active area of the DMOS design was also not of critical importance to the SSPC requirements again due to the highest priority of table 2.1 being placed on reliability. With this in mind then the DMOS NPT device type seemed the best choice out of the IGBT types studied for use in an SSPC as it had proven high ruggedness against short circuit failure and hence any slightly increased static conduction losses could be compensated for in the event of a short circuit. In addition the NPT IGBT die could be more easily placed in parallel and would require less protection circuitry therefore a reduction in mean time to failure (MTTF) would result due to the inherent simplifications.

2.3.6 Anode shorted IGBT type of bipolar devices

One additional development in IGBT technology was the incorporation of an anode shorted structure to form a Reverse Conducting IGBT (RC-IGBT), the first documented development was called the LightMOS by Griebel[63] as shown in figure 2.8. The purpose

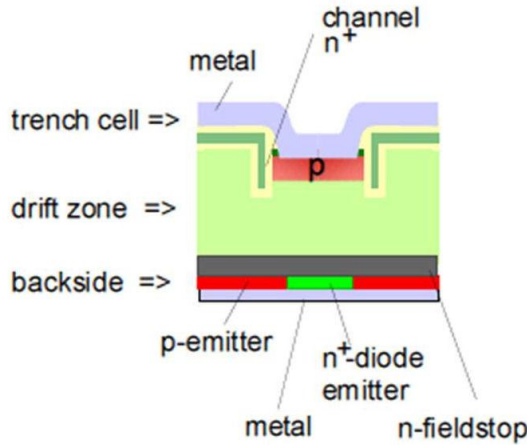


Figure 2.8. The “LightMOS” or Reverse Conducting IGBT, as depicted by Griebel[63].

was to integrate an anti-parallel diode into the IGBT structure to avoid the use of an additional diode in the cost sensitive lamp ballast application. The initial idea was developed further by Voss[64] for higher power applications (600 V) as it was found that the RC-IGBT could turn off a load much faster than a conventional continuous, or solid, anode IGBT. the benefits of using the RC-IGBT in comparison to conventional IGBT devices was described by Chiola[65] where the turn off energy was substantially lowered by this development and the switching speed was raised to 100 kHz (from 20-40 kHz) due to reduced charge storage. One of the new generation devices at Infineon which replaced the IGP30N60T[60] at 600 V rating was the high speed 3 generation IGP30N60H3[66]. Eventually Voss[67] achieved a 1200 V RC-IGBT device with an optimised anode structure to reduce the issue of ‘snap-back’ which otherwise worsened with increased drift region length. Snap-back occurred when the bipolar conduction activated at a given level of V_{AK} bias. The bipolar activation, or start up voltage (V_i) for the normal IGBT was around 1 V, but for the RC-IGBT this was larger ($V_i=1.5$ to 2 V) but, once conducting the voltage level across the terminals snapped

back to around 1 V. In 2009 Rahimo[68] developed the Bi-mode Insulated Gate Transistor (BiGT) concept based on the RC-IGBT, and it was argued by Storasta[69] that the BiGT concept removed the possibility of snap-back in larger BV rated devices and hence provided an improvement over RC-IGBT through optimisation of the respective areas of the P-Anode of the IGBT and anti-parallel N^+ cathode of the integral diode as shown in figure 2.9.

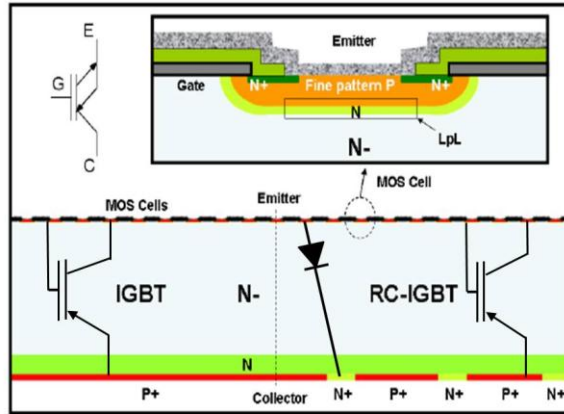


Figure 2.9. The BiGT concept, as depicted by Rahimo[68].

2.3.7 Introduction of Charge balanced devices

One final and game changing technological breakthrough, which enabled silicon devices to reach higher BV ratings and yet achieve reduced on state static conduction loss, was the development of charge balance theory as first proposed by Fujihira[70, 71], creating what is known as Super Junction (SJ) device. The idea was exploited by Infineon within their CoolMOS MOSFET product line, as described by Deboy[23]. The idea enabled both a vertical and lateral electric field of equal magnitude to be developed in the drift region which meant that the drift length could be much reduced which enabled lower on state loss. In addition the use of charge balance enabled a higher doping in the N-Drift region which enabled further reduction in on state loss for the unipolar MOSFET class of devices. The switching speed of the CoolMOS device was also reduced in comparison to a DMOSFET while still using the now standard trench gate to reduce the cell width and improve the channel width to cell width ratio. Thus the CoolMOS MOSFET range offered the lowest

$R_{(ON,SP)}$ of any MOSFET, but the BV was limited to 900 V [72], and it could be argued that 600 V was the effective limit of the charge balance benefit, thereafter an IGBT was most suited to lowest static conduction loss. The voltage rating limit within a CoolMOS was due to the Aspect Ratio (A/R) of the columns as described by Sakakibara[73]. Essentially, the pitch of the columns in ratio to the length of the columns provided the A/R. Due to manufacturing constraints the depth limited the achievable pitch and hence the A/R. The structure of the CoolMOS type of MOSFET and the effect of A/R can be seen in figure 2.10, reproduced from Sakakibara[73]. In this case the one dimensional (1-D) silicon limit line was based on trench gate devices which, due to the increased packing density, achieved a lower $R_{(ON,SP)}$ than the DMOS, as described by Zingg[74]. Clearly from figure 2.10 with a high enough aspect ratio then extremely low $R_{(ON,SP)}$ could be achieved at high BV , but thus far this has not been achieved in manufacture. As a comparison working in 2006 Saito[75] achieved an $R_{(ON,SP)} = 15.5 \text{ m}\Omega\text{cm}^2$ at 680 V with an aspect ratio of about 10. Later in 2008 a trench gated MOSFET was developed from Infineon[22, 72] first at $BV=600$ V then at 900 V, which are shown in figure 2.10 to provide a realistic commercial capability which achieved an aspect ratio of around 20-25. Thus, the comparison provided in figure 2.10 indicated the rapid improvement in process technology.

In addition to the pitch, the BV of the super junction type device was also dependent upon the charge contained in the alternating N and P columns, any variation from the design target during manufacture leads to rapid reduction in the achieved BV as described by Saito[75] as shown in figure 2.11. If a large BV was required and yet the desired A/R and pitch could not be manufactured then a semi-super junction device structure was possible (Semi-SJ) again as described by Saito[76] which used a normal N-Drift region (called a bottom assist layer) of a given length to supplement the charge balanced drift region.

As stated earlier the development of the MOSFET and IGBT are linked, it was inevitable therefore that the SJ idea as used in MOSFET technology would transfer into IGBT technology. To that end Antonio[77, 78] created the Super Junction Bipolar Transistor (SJBT). In DMOS form this structure is compared to a DMOS Field Stop PT IGBT

(FSIGBT) as shown in figure 2.12. In effect this was a vertical super junction insulated gate bipolar transistor which again used super junction techniques to minimise the drift length and reduce the PNP BJT base width, which effectively was the N-buffer width (instead of the N-buffer width plus the N-Drift length for the FSIGBT). In this case however, the carriers travelled separately in the respective columns (electrons in the N column, holes in the P column), thus providing reduced charge storage, thus increased switching speed, enabling latch up free operation and much reduced turn off losses in comparison to the non charge balanced FSIGBT. The only negative point was that a 9 % increase over the FSIGBT in terms of bipolar activation voltage (V_i) occurred in the SJBT, thus the on state voltage V_{AK} was increased.

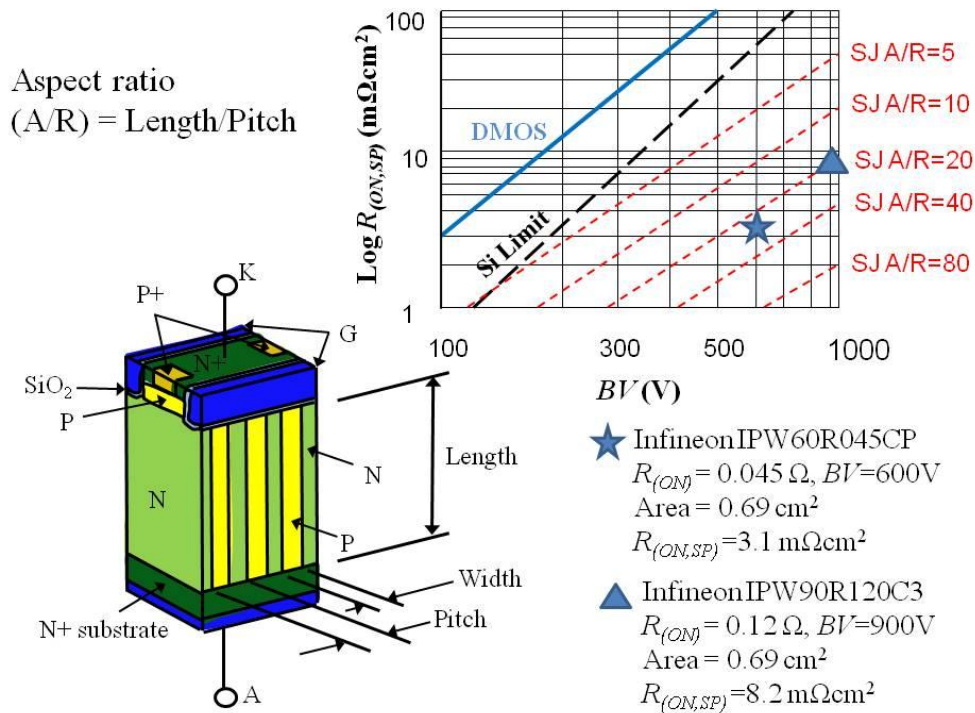


Figure 2.10. Trench gate charge balanced MOSFET and effect of column aspect ratio. Using data from Sakakibara[73] and Infineon[22, 72].

Antonio[79] also adapted the SJBT to trench gate technology and incorporated the anode shorts of the RC-IGBT in order to remove the snap back effect of that device and further reduce dynamic losses, following on from the work of Voss[64, 67]. At the time of

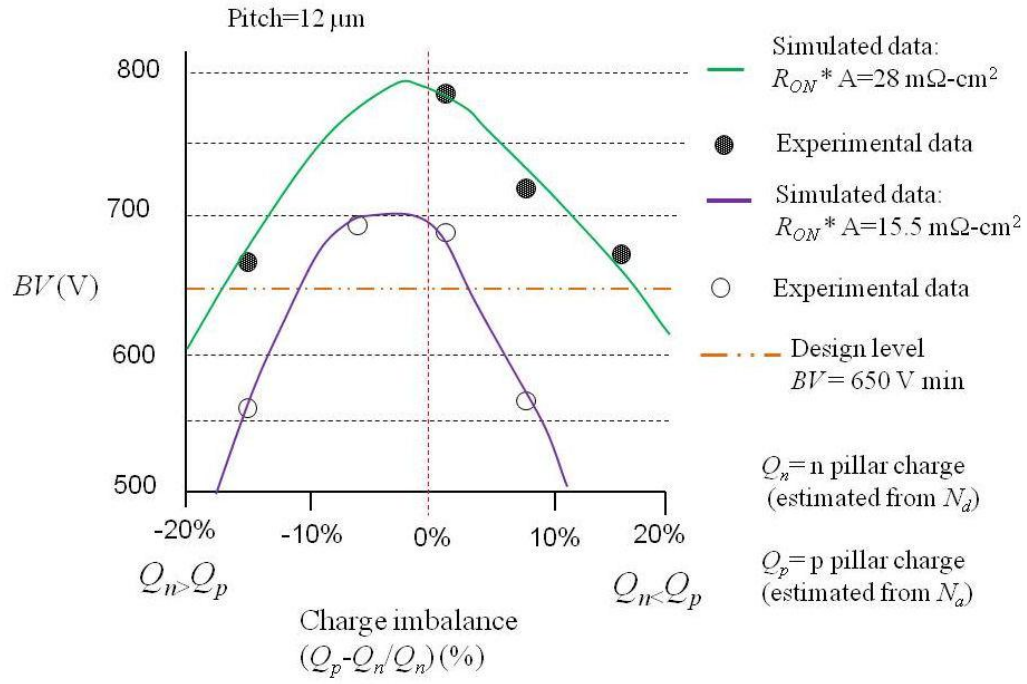


Figure 2.11. Effect of charge imbalance on BV , as depicted by Saito[75].

writing however, all the data from the work of Antoniou[77-79] had been on computer simulations, but if exploited could prove a promising technique to obtain reduced dynamic losses and improved reliability.

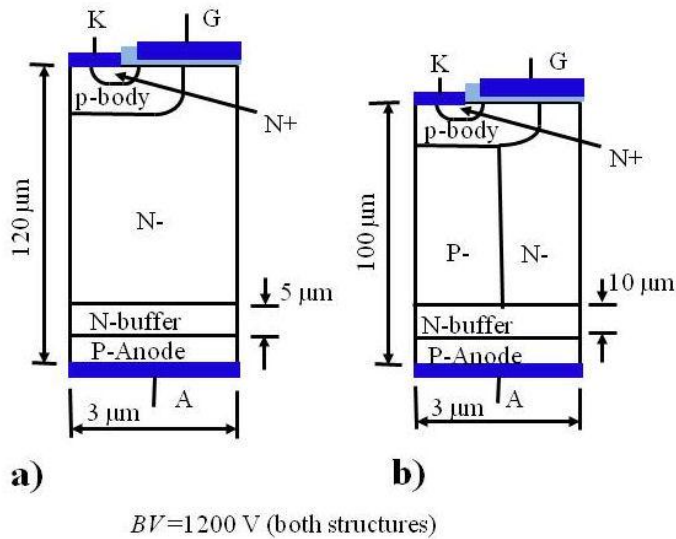


Figure 2.12. Comparison of a) DMOS Field Stop IGBT and b) DMOS SJBT, as depicted by Antoniou[77, 78].

As described by Sorrentino[80] of ST Microelectronics their version of the super junction MOSFET (called “MDmesh”) also provided the same benefits to loss reduction as the CoolMOS. However, Sorrentino pointed out that the use of wide band gap semiconductor products in a system, such as a silicon carbide (SiC) diode, in the absence of a commercially available wide band gap switching device, could further reduce the overall system losses during inductive load switching.

2.3.8 Summary of silicon devices

Tables 2.2, 2.3 and 2.4 are provided below in order to summarise the performance of all the silicon devices reviewed in section 2.3. Table 2.2 shows both the relative merits and demerits of the silicon unipolar device types. While table 2.3 shows the relative merits of the bipolar device types and table 2.4 shows the relative demerits.

	Merits			Demerits		
VDMOSFET	Fast switching when compared to bipolar devices (IGBT/BJT) $t_{off} < 10$ ns	Low current density in channel area= increased ruggedness	Rugged, low current density design	Increased static loss when compared to IGBT		
UMOSFET	Same benefit of VDMOSFET but reduced cell width	Increased channel area to cell width ratio= reduced $R_{(ON,SP)}$	Low dynamic loss	Increased static loss when compared to IGBT	Increased current density-reduced ruggedness	
Super Junction UMOSFET	Reduced drift length for a given BV = reduced $R_{(ON)} \leq 0.45 \Omega \text{cm}$ @ $BV=600$ V	Extremely fast switching ≤ 5 ns	Monitor V_{AK} to predict failure (increases for given current)	Increased static loss when compared to IGBT but reduced in comparison to VDMOSFET & UMOSFET	Complex manufacturing process with unique A/R limitations on BV and charge balance	Switches too fast resulting in higher E_{off} with inductive loads and potential for body diode avalanche

Table 2.2. Summary comparison of the relative merits/demerits of unipolar silicon devices.

Current control	BJT's	Fastest switching bipolar device $t_{off} < 1 \mu s$, especially with Baker clamp to remove stored charge.				
	Thyristors	Lowest on state loss at high BV ($V_{AK} = 1-2$ V at 6 kV)				
	Gate Turn Off Thyristor (GTO)	gated turn-on and turn-off capability				
Voltage control	MOS controlled Thyristor (MCT)	High BV , low on state loss, high saturation current	Voltage control via MOS gate			
	Emitter Switched Thyristor (EST)					
	NPT-IGBT DMOS	Assymetrical BV rating, suited to 1.5 kV and up	Increased ruggedness over DMOS PT-IGBT and UMOS FS-IGBT	Reduced toff time compared to PT and FS type IGBT due to drift and diffusion current mechanisms operating	Flat current reponse after short circuit, increased short cicuit withstand time	
	PT-IGBT DMOS	Increased current gain over NPT IGBT				
	Field Stop UMOS PT-IGBT	Increased saturation current levels compared to PT-IGBT	Thinnest W_B of any IGBT for a given BV_{CEO} , highest current gain	Reduced cell width as compared to DMOS type NPT & PT IGBT- reduced silicon area for given current.	Highest controllable current IGBT	Reduced parasitic JFET effect as compared to DMOS IGBT types
	RC-IGBT/BIGT	Anode shorted design provides built in parallel diode function	Build in diode allows reduced t_{off} in comparision to other IGBT types.	Reduced susceptibility to latch up.		
	UMOS SJ-IGBT	Reduced W_B for given forward BV rating as compared to FS-IGBT= increased current gain	Latch up free design			

Table 2.3. Summary comparison of the relative merits of bipolar silicon devices.

Current control	BJT's	Approx 500 V max BV	High base drive current due to low current gain		
	Thyristors	High gate current drive	requires commutation or power down to turn off.	150 μ s turn off	
	Gate Turn Off Thyristor (GTO)	High gate current drive	Gate current required to be maintained after turn on	15 μ s turn off	high forward voltage in comparison to thyristor ($V_{AK} = 3$ V at $BV=4$ kV)
Voltage control	MOS controlled Thyristor (MCT)	Higher dynamic loss than IGBT due to increased charge storage	Max controllable current restricted		
	Emitter Switched Thyristor (EST)	Reduced saturation current as compared to IGBT and MCT	similar poor turn off times and high dynamic loss as MCT's	Increased complexity due to dual gate design	
	NPT-IGBT DMOS	Lower current gain than PT IGBT (wider W_B)	Subject to latch up		
	PT-IGBT DMOS	No reverse BV	Subject to latch up	Irradiation required to decrease charge storage/turn off loss	Reduced short circuit withstand time in comparison to NPT IGBT
	Field Stop UMOS PT-IGBT	Reduced ruggedness as compared to DMOS IGBT types due to increased current density	Increased latch up susceptibility due to increased hole current	Reduced short circuit withstand time in comparison to NPT IGBT	Short circuit current continues to increase until thermal failure
	RC-IGBT/ BIGT	'snap back' effect increasing with BV rating, requiring anode area/shape optimisation	Subject to latch up		
	UMOS SJ-IGBT	Increased bipolar start up voltage (V_i) in comparison to FS-IGBT	Complex manufacturing process with unique A/R limitations on BV and charge balance		

Table 2.4. Summary comparison of the relative demerits of bipolar silicon devices.

2.4 Wide band gap devices

The benefits of wide band gap materials such as silicon carbide (SiC) gallium nitride (GaN) and diamond, as a specific form of carbon (C), have been long discussed as summarised by Hudgins[81] in terms of their current capacity and dielectric performance. Hudgins[82] also reviewed the material choice from a power semiconductor device perspective, indeed the relative benefits of many semiconductor compounds to unipolar devices were directly compared by Chow[83], both concluded that GaN was the best material for unipolar devices with high mobility (low on state loss) and high dielectric strength. Diamond however, was recommended by Hudgins as the best material for bipolar devices due to high electron and hole mobility and very high thermal conductivity ($\lambda = 600\text{-}2000 \text{ W/mK}$). In general the use of wide band gap materials to make power semiconductor devices offered an increased critical field and higher electron mobility than silicon, thus give rise to reduced drift length and hence low static on state loss and low dynamic loss switching devices. SiC, in various poly type forms: 3C, 4H, and 6H, and GaN, however, have become the main focus of researchers as the processing of the materials differs markedly from that of silicon. Most apparent is the cost and quality of the wafer materials. All wide band gap semiconductors involve vapour phase crystal growth, thus to reduce material cost layers were grown on to a substrate, which in GaN prevented fabrication of vertical devices until recently when single crystal (bulk) wafers became available as described by Kachi[84]. Kachi went on to compare and contrast the benefits of vertical and lateral device structures in GaN and SiC. The cost of a vapour phase grown layered substrate wafer is 2 magnitudes higher than silicon as described by Kaminski[85], however a new material was required to overcome the material issues of silicon in order to reduce losses further for a given BV rating. Indeed, Kaminski[85] described the competing silicon technology of the super junction concept as a “workaround”. Kachi[84] concluded however, that the cost performance benefits of the available wide band gap devices needed improvement in order to gain widespread usage and displace silicon super junction devices in $<1000 \text{ V}$ rated applications as required for high volume automotive

manufacturers. This was supported by Kaminski[86], stating that the best GaN devices would be fabricated on GaN bulk crystal material, but the cost of the currently available 2” wafer form was around 100 Euros/cm², whereas bulk SiC was 10 Euros/cm² on 4” and recently 6” wafers, thus lending itself to device cost reduction.

The properties of the targeted wideband gap materials are shown in table 2.5. The main benefits of using wide band gap materials for semiconductor devices was summarised by Kaminski[87] and Hudgins[82]: such that the drift length was much reduced by the high critical field, thus obtaining lower losses at very high *BV* rating. Leakage current at high temperature was much reduced due to the lower intrinsic carrier concentration of the wide band gap materials and the ability to work at high lattice temperatures is also attractive to minimise heat sink size requirements. The dynamic, or switching, losses were also lower in wide band gap materials than silicon and hence they were attractive for high frequency

Parameter	Silicon	4H-SiC	GaN	Diamond
Band-gap E_g (eV)	1.12	3.26	3.39	5.47
Intrinsic Conc. n_i (cm ⁻³)	1.4E10	8.2E-9	1.9E-10	1E-22
Critical Field ε_{crit} (MV/cm)	0.23	2.2	3.3	5.6
Electron Mobility μ_n (cm ² /Vs)	1400	950	1500	2200*
Hole Mobility μ_p (cm ² /Vs) *	450*	50*	10*	1800*
Permittivity ε_r	11.8	9.7	9.0	5.7
Thermal Cond. λ (W/cmK)	1.5	3.8	1.3	20
BFoM: $\varepsilon_r \cdot \mu_n \cdot \varepsilon_{crit}^3$ rel. to Si	1	500	2400	9000

Table 2.5. Properties of wide band gap semiconductor relative to silicon (Kaminski[85],*Hudgins[82]); BFoM = Baliga Figure of Merit.

switching applications where dynamic losses become more important than static losses as described by Chow[83].

The choice of GaN or Silicon carbide materials for power devices as at 2012 was summarised by Kaminski[86] who stated that GaN was most suited for high frequency discrete devices and Integrated Circuits (I.C.s) of 1000V rated devices with current capability up to a maximum of 10's of Amps, whereas SiC was most suitable for vertical power devices with no current limitations with $BV > 1000$ V. However, in terms of $R_{(ON,SP)}$ versus BV plots then GaN potentially has the capability to achieve the lowest loss for highest BV rating as demonstrated in the provided by Hilt[88], as reproduced in figure 2.13. Currently the only device type in which both GaN and SiC materials compete directly is in the Schottky type devices, then according to Kaminski[86] the choice is down to relative unit cost.

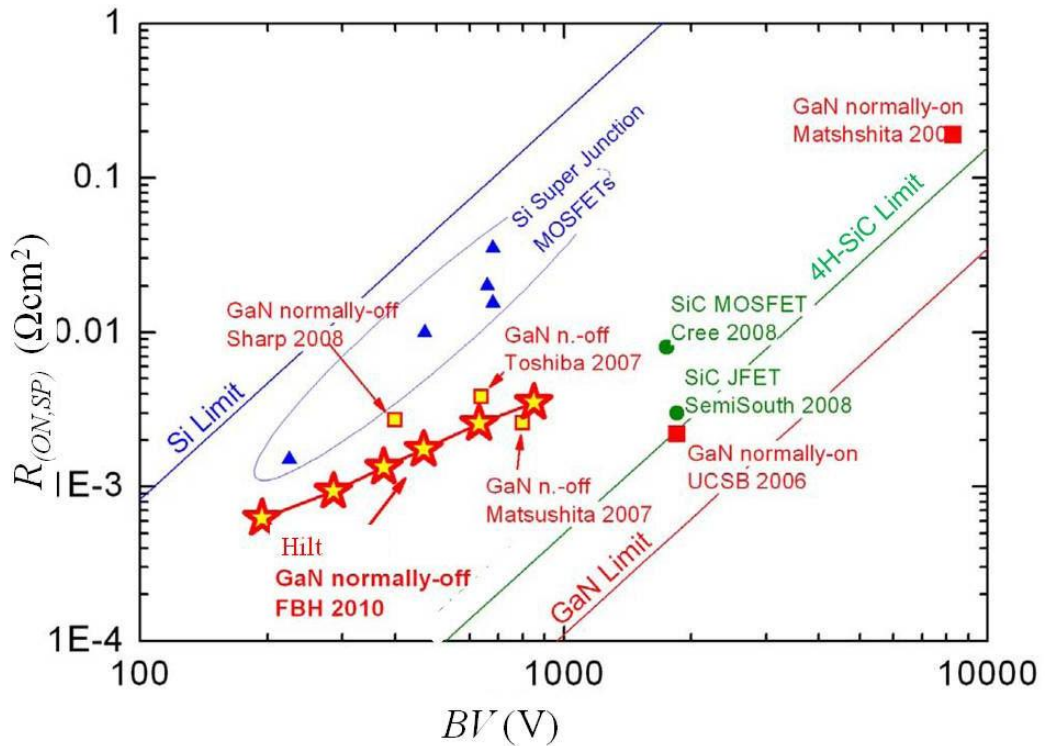


Figure 2.13. Specific on state resistance versus BV rating: comparison for a selection of unipolar devices fabricated in GaN and SiC as compared to silicon super junction types. Hilt[88].

2.4.1 Silicon Carbide (SiC)

Although the benefits of using SiC devices are many, as described by Agarwal[89], and supported by Kaminski[85] and Chow[83]. The problems associated with manufacturing semiconductor devices were not trivial, for example to form a unipolar MOSFET in SiC then

the oxide interfacial layer included carbon clusters within it which degraded the mobility below that possible in theory, as summarised by Kaminski[85] and Matocha[90]. Therefore unipolar devices such as MOSFETs to date have not achieved their theoretical performance and have been disappointing in proportion to their high unit cost (the cost-performance compromise, Kachi[84]). Adoption into system designs therefore had been slow. Material supply was a large contributory factor as to why SiC MOSFETs had yet to make a contribution in widespread commercial applications. Wafer supply currently was limited by defect densities, to date only 4" diameter material was available, but 6" had been promised by Cree[91] with minimised defects. Previous fears about oxide reliability had been alleviated as described by Yu[92] and were no longer considered to be an issue.

An alternative unipolar switching device is the JFET type, this type did not suffer from any oxide interface issues and were readily available in SiC material from Semi South Inc, as described by Sheridan[93]. Previously these suffered from being a normally on device, thus they required a Cascode configuration to offer a normally off switch capability. However, a new normally off JFET device was obtained which achieved an extremely low $R_{(ON,SP)} = 2.8 \text{ m}\Omega\text{cm}^2$ at a $BV=1200 \text{ V}$, and have been proven to demonstrate low dynamic loss as described by Kelley[94]. Ostling[95] though indicated that the operational threshold voltage of the normally off SiC JFET was limited, and that the operating temperature range of the JFET may also be limited. A successful demonstration of the JFET, in replacement of a silicon IGBT, was shown to improve the efficiency by 1 % of a photovoltaic inverter as described by Mazolla[96]. Unfortunately, most of the data describing successful usage of the SiC JFET had unfortunately come out of Semi South however, one independent SSPC design was demonstrated by Handt[97] which successfully used a SiC JFET in Cascode configuration to provide normally off operation. The SiC JFET does however, provide excellent predicted reliability as the structure is based purely on a P-N junction technology and although not of importance to this SSPC application, the JFET devices are high switching speed capable according to Ostling ($>100 \text{ kHz} < 200 \text{ kHz}$).

As to the use of SiC for bipolar devices then Ostling[95] provided a good summary of each reported device type: such as BJT, GTO's and Thyristor. Ostling however, did not mention the IGBT type presumably due to the channel mobility issue, although some IGBT results have been reported such as the p-channel IGBT described by Zhang[98], but attempts to create what in theory should be a lower loss N channel IGBT were hindered by the high resistance of the available P type substrate material in SiC, as required to form the P-Anode, indeed the resistivity was in the region of (0.8 to 1.0 Ω cm) according to Wang[99]. To overcome this limitation a free standing N channel IGBT was produced by Wang[99] on an n-type substrate where all the layers required were grown in a continuous sequence and subsequently the substrate was removed to leave 180 μ m thick free standing SiC into which an N channel IGBT was fabricated with $BV=20$ kV and $R_{(ON,SP)} = 177$ m Ω cm², a current density of 27.3 A/cm² was reported. In comparison an n-type IGBT formed on high resistance p-type substrate described by Das[100] provided a device of half the blocking rating (10 kV), but a current density of 100 A/cm². A fundamental issue unfortunately affected bipolar devices, as fabricated from SiC, due to the forward voltage instability caused by movement of the basal plane stacking faults as described by Sumakeris[101].

2.4.2 Gallium Nitride (GaN)

According to Hudgins[82] the use of GaN for bipolar device was not possible due to the very low hole mobility, therefore only unipolar devices were possible as electron mobility was higher than Silicon as shown in table 2.5. Such unipolar devices according to Kachi[84] were suitable for automotive applications and had investigated both vertical and lateral device types. The cost performance of GaN however, according to Kachi, was in need of improvement. Germain[102], Brier[103] and Ueda[104] expressed that GaN layers grown on silicon offered an improved cost performance which could challenge silicon super junction devices. Other substrates included sapphire or SiC to ensure good coefficient of thermal expansion match, but all required some form of buffer layer. SiC substrate in particular enabled high temperature operation of the GaN based High Electron Mobility Transistor

(HEMT) devices as described by Maier[105], but the buffer layer between the materials in all cases (GaN to SiC, sapphire or silicon) was key to prevent mechanical stress and hence failure of the device. For example Selveraj[106] stated that a thick aluminium nitride (AlN) buffer layer was key to the achievement of an equivalent electron mobility in a GaN layer grown on silicon, (separated by the buffer) as compared to a layer grown on SiC or sapphire.

The most common class of device, due to the cost of bulk material, was the Lateral HEMT available up to a rating of 1000 V. These however, were normally on devices and although much work had been done to fabricate normally off devices, no successful design had emerged as yet. Attempts included using a fluoride based plasma to adjust the threshold voltage (V_{TH}) from depletion mode to enhancement mode, alternatively a recessed gate structure could be used with an MIS (Metal Insulator Semiconductor), as described by Saito[107], but both achieved a very low threshold of ($V_{TH}<+1$ V) according to Hilt[88]. Hilt instead utilised a P type GaN gate to deplete the GaN channel layer to provide an enhancement mode HFET, however the resultant device still had a high leakage current of $4\text{E-}6$ A/mm at $V_{GK}=0$ V. According to Kachi[84] the current drop off during switching of the HEMT was also a major problem. Saito[108, 109] stated that the current collapse was due to electron trapping in the AlGaIn/GaN layers, the charge of which depleted the two Dimensional Electron Gas (2-DEG) channel. Briere[103] reported that for devices of $BV=600$ V then this problem had been eliminated.

An alternative structure was the GaN MOSFET which used an MIS gate of either silicon dioxide (Matocha[110]), or high k dielectric layers (Tsai[111]) to provide increased V_{TH} , but both still suffered from high leakage at $V_{GK}=0$ V and a low sub threshold slope.

2.4.3 Diamond

As regards diamond then although this material in theory would provide ideal semiconductor switches as described by Schneider[112]. Unfortunately, although the material has the highest hole mobility of any semiconductor material the material would not accept n-type

doping into its crystal lattice again as described by Schneider[112]. In fact only boron (B), an acceptor; nitrogen (N) and phosphorous (P), as donors, can be used as dopants, but each (especially the donors) has a high activation energy and so does not achieve ionisation at room temperature as described by Kohn[113].

Due to the inability to form a P-N junction a photo-conductive or electron beam switch were trialled by Schneider, but both achieved low efficiency. It followed that manufacturing a device in diamond was dependent upon conduction by thermionic field emission. To date a Schottky diode had been demonstrated by Brezeanu[114], but the on state voltage drop was very large due to the very low intrinsic carrier concentration and the achieved current density was low (100 A/cm^2). Even the simplest of structures such as the edge termination was difficult to achieve in diamond currently as reported earlier by Brezeanu[115].

2.4.4 Summary of wide band gap devices

A summary of all wide band materials discussed above as related to power semiconductor devices was documented by Millan[116] in 1997, which included switching devices.

Although, much research work has occurred in the period since that date the findings and conclusions are still equally valid in 2012, but much improvement has occurred in the period since 2008 in the quality of materials for example (6" SiC wafers are now available).

The unipolar switches in SiC (MOSFET devices) have now been made available by Cree[91], but are very costly and have disappointing performance, they do however a performance improvement over silicon MOSFETs in terms of $R_{(ON,SP)}$ versus BV , as shown in figure 2.13, albeit for a factor of 10 times the cost of silicon MOSFETs. GaN device types thus far, for power switching applications, are still struggling to meet adequate current per unit area targets and again the bulk material is expensive compared to both Si and SiC. As to diamond again, the device type only seems to be able to offer Schottky type operation where the competing material SiC is relatively strong.

As to bipolar switches then these are only possible in SiC unfortunately, these suffer from forward voltage instability which includes IGBT types.

2.5 Other technologies

In the absence of good cost performance, commercially available, wide band gap switching devices with a BV rating of between 600 V to 1200V with high current density then the use of standard silicon devices remained the only viable option. This section reviews the options in the case where a single switching device class operating alone cannot satisfy the requirements of the SSPC.

2.5.1 Modular construction IGBT-MOSFET parallel circuit

In this case the only way to obtain a semiconductor switching device with lowest on state loss under all conditions (both static and dynamic) was to use a parallel IGBT and a MOSFET as described by Kimball [117] as shown in figure 2.14. The parallel devices were to be assembled into a power module type construction as shown in figure 2.15. In this case the low nominal current is conducted via the MOSFET and the high fault or surge current is conducted through the IGBT. This system thus avoided entry into the saturation region of the MOSFET characteristic (provided that the active area is calculated correctly) and yet

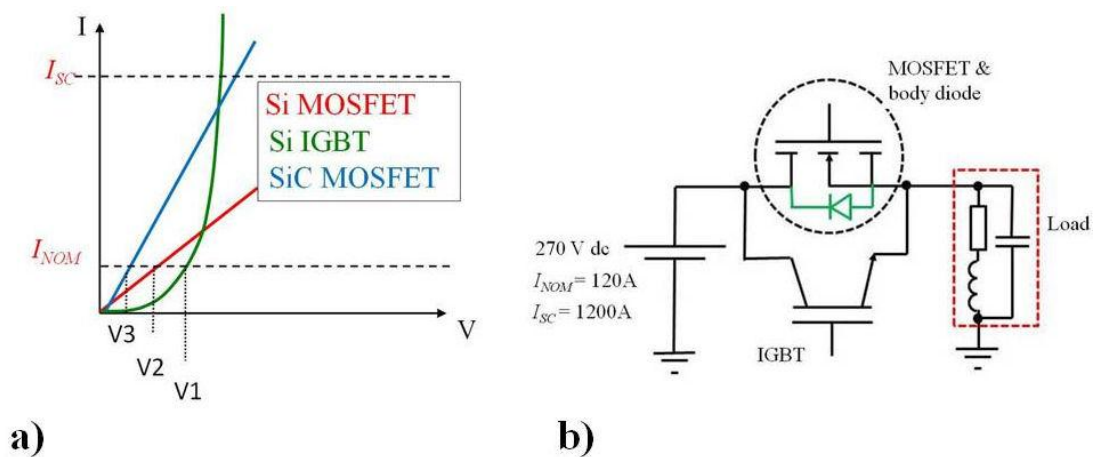


Figure 2.14. Proposed hybrid for lowest losses under all conditions: a) comparison of generalised forward I-V characteristics (gate voltage $\gg V_{TH}$), b) schematic representation of the hybrid.

provided lowest loss switching of the nominal current. The necessary forward voltage drop to bipolar start up (V_i) within the IGBT is avoided by having the available MOSFET conduction and yet the IGBT has the lowest conduction loss at high fault current and hence a reduced active area is required of the MOSFET in order to conduct the anticipated fault current. The IGBT however, still suffered from a tail current and hence the resultant high dynamic loss when turning off the fault current.

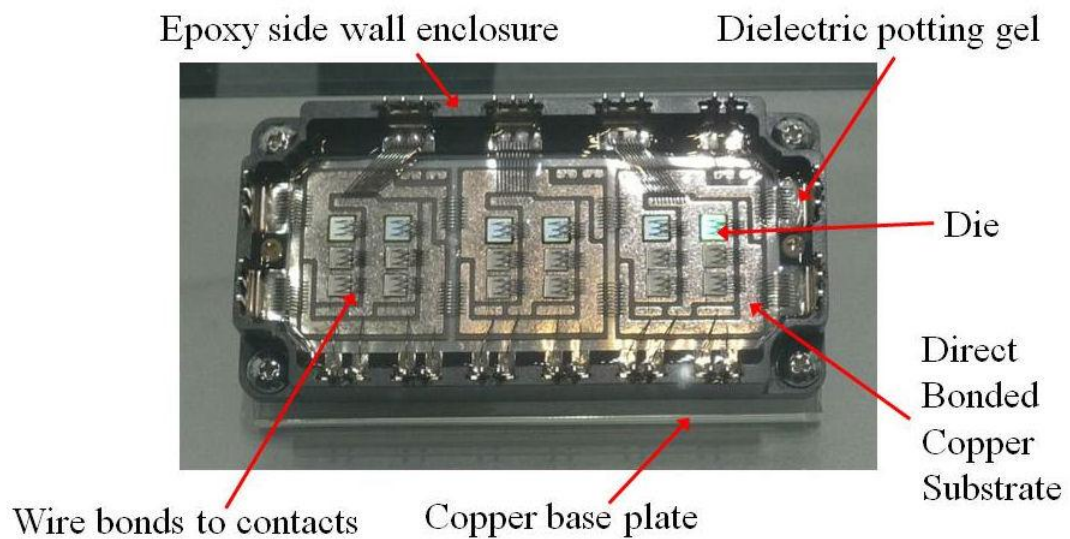


Figure 2.15. Typical “chip and wire” power module assembly (Denso Corporation).

The drawback of this parallel technique was the gating requirements as described by Kaerst[118] regarding when ambient heat sink temperature and self heating are taken into account due to the changing forward I-V characteristics with temperature, which will alter independently within each type. For example the MOSFET on state loss will increase with increased temperature, but the IGBT may not. At least the increased switching losses due to increased switching frequency can be ignored for the SSPC application. To reduce the turn off losses of the modular hybrid an Application Specific Integrated Circuit (ASIC) was designed specifically to provide the gate drive function of a parallel IGBT and MOSFET (Yee[119]) the aim was to ensure that the IGBT was gated off first while the MOSFET conducted to reduce the turn off loss, the faster MOSFET was subsequently then gated off once the current had reduced via the gate control of the IGBT. This ASIC also adjusted the gating to the individual device classes in accordance to the ambient heat sink temperature

characteristics in order to minimise static loss. The gate control was therefore very complex and not simply a question of connecting the gate terminals together of the MOSFET and IGBT. The work of Hoffmann[120] emphasised the use of IGBT and MOSFET die which were fastest in class to minimise dynamic losses, but highlighted the effect of IGBT conductivity modulation as limiting the upper limit of the switching frequency.

Unrelated to the upper switching frequency, but instead to ensure highest reliability then the use of matched die was also critical to the parallel hybrid as described by Bontemps[43]. If using multiple die of both classes (MOSFET or IGBT) then the threshold voltage (V_{TH}) and transconductance (g_{mL}) should be matched as a minimum over the ambient heat sink temperature range. Under two types of short circuit:- fault under load, and hard switching fault Musumaci[121] identified that the modular power tile layout was a major influence on parallel IGBT current share, relating to the individual device characteristics, over the ambient heat sink temperature range. This was due to stray parasitic elements as part of the layout as described by Abbate[122] such as gate resistance, inductance and capacitance which resulted in instability and ultimately in failure that looked like dynamic avalanche. In particular Basler[123] considered asymmetries of the gate resistances which caused unequal current share through parallel IGBT devices during inductive turn off which resulted in different gate capacitance discharge times again causing failure in individual IGBT devices which subsequently escalate to cascade failure. Eckel[124] also described the importance of the gate resistance to the turn off performance of the IGBT due to uneven discharge of the gate capacitance causing hotspots. To prevent unequal current share Lobsinger[125] proposed using a dedicated gate control and current/voltage sense for each paralleled IGBT. This proposed system was related to that proposed for matrix control of IGBT devices by Palmer[126], but both solutions were costly, suffered decreased Mean Time To Failure (MTTF) due to the added complexity and added weight to the overall SSPC design.

2.5.2 Reliability of the compared MOSFET and IGBT silicon devices

With regard to the key requirement of reliability then the work of Saint-Eve[127] used a long term campaign to determine the number of short circuit conduction or avalanche events which could be repeated without detriment to the CoolMOS device performance. The work was also compared directly to an NPT IGBT of similar voltage rating; all devices were in the TO247 standard epoxy package. Under avalanche conditions then the CoolMOS critical dissipated energy was found to be 1.5 Joules at 25°C (300 K) and 0.95 Joules at 125°C (≈ 400 K). Prior to reaching the critical energy level the avalanche tests could be repeated, indeed under continuous testing, one CoolMOS device survived over 9500 avalanche tests at 125 °C when the avalanche energy was kept below the critical limits. The dissipated energy was set by the inductance value of a given load and the starting current through it prior to gate turn off. In repetitive short circuit testing again at 125 °C (where low mobility provided highest resistance) then the number of short circuit events survived was 10,000 provided that the short circuit energy was kept below 1.25 Joules, beyond that energy level the device failed instantly. The energy level was set by the applied voltage and short circuit current which was limited to 400 A. The forward voltage across the device was shown to provide an indicator as to a life failure as the V_{AK} rose progressively after 10,000 short circuit events if the energy was kept below the critical value. Using the same short circuit test rig, the comparison NPT IGBT demonstrated a critical energy level of 0.65 Joules at 125 °C and 0.82 Joules at 25 °C, which was lower than the CoolMOS device, again failure occurred instantly if the critical energy level was exceeded. For short circuit energies kept below the critical energy level then $>10,000$ operations could be achieved.

As regards the causes of life failure (after approximately 10,000 operations) the continued work of Lefevbre[49] followed on from the work of Saint-Eve[127] to determine that no measured parameter on the NPT IGBT provided any indication of end of life which contradicted the work of Eckel[61]. This was unlike the CoolMOS wherein the forward volt drop provided an indication of life failure. The failure mechanisms in all devices tested were

described as a “cumulative damaging mechanism”. The related work of Arab[128] (although conducted on trench gate field stop IGBTs) confirmed the “cumulative damaging mechanism” was due to degradation of the Aluminium metallisation leading to increased resistance, cracking and bond wire lift off. The IGBT in the work of Lefebvre[49] was subject to delayed turn off failure where the device appeared to turn off only to fail approximately 700 μ s after turn-off was applied to the gate due to stored charge leading to destructive thermal runaway. These findings thus support the choice of Ahmed[20] to use the CoolMOS type MOSFET devices in the SSPC design of sufficient active area to maintain operation in the liner region at the fault current level.

The work of Roig[129] however, compared the thermal behaviour of VDMOSFET and CoolMOS type MOSFETs under short circuit conditions. Due to the lower current density for the VDMOSFET (requiring larger active area than the trench gate CoolMOS type devices) then the time to fail due to short circuit current was much longer than that of the CoolMOS. In all cases however, time to failure after incidence of short circuit current was always greater than the 10 μ s required to detect the current and turn off the device.

2.6 Choice of switch technology for highest reliability SSPC

To conclude as regards a selection of the technology to be investigated within this research work for use in the SSPC then in the absence of a suitable wide band gap switching device then a silicon solution needed to be investigated such as the use of super junction MOSFETs to meet the minimum requirements of $BV= 500$ V. The silicon device would serve in the short to medium term applications, but when commercially available, with the necessary cost performance benefits, then a unipolar SiC MOSFET device could potentially replace silicon in the longer term. The use of SiC devices throughout the MEA may allow an increase in system voltage to ± 400 V dc (or higher) and hence enable further weight saving in cables and hence added fuel efficiency.

A common theme in the evaluation of the silicon MOSFET and IGBT technologies was that the DMOS type construction offered increased reliability against short circuit and avalanche failure due to the reduced current density and electric field around the gate electrode (where the device lattice temperature is highest). This feature provided for the ability to sustain fault current conduction for a longer period of time and for a higher number of repetitions provided that sufficient active area was available to maintain current and voltage levels at all times within the critical energy limitations of the device. The trench gated technologies utilised in CoolMOS product and recent generation field stop (PT) IGBTs reduce the active area required for a given current level, offering improved cost performance benefit, via an improved specific on state resistance, $R_{(ON,SP)}$, versus BV performance. These trench gate devices however, were not considered as rugged as the preceding generation of VDMOSFET or DMOS NPT IGBT type devices by academic peers, which cut through the marketing campaigns of individual companies aiming to promote their current product line. Despite using a trench gate the CoolMOS product however, was independently proven to be more rugged than an NPT IGBT of equivalent BV by Lefebvre[49] and the forward volt drop of the CoolMOS device could be monitored to predict end of life. The CoolMOS type device therefore, provided that the fault current was fully characterised and the largest current predicted, could be used to provide reliable switching if enough active area could be provided to maintain operation in the linear region. However, a conservative margin for error was required in that predicted fault current, especially when using Li-Ion batteries may be necessary.

A parallel modular construction was shown to provide, via an IGBT, a means of offering short circuit protection to a limited active area of MOSFET. If a parallel construction was to be used, and silicon area was a critical concern, then the use of CoolMOS devices (of sufficient area to conduct a nominal load current) would be sufficient if a DMOS NPT IGBT could be utilised in parallel within the SSPC design. However, to avoid inhomogeneous operation of the multiple gates, leading to uneven current share, and

to avoid the complexities of separate gate timing, between the MOSFET and IGBT class devices, then potentially the most reliable alternative would be to create an injected VDMOSFET with a built in, self biased minority carrier injector on a single active area of silicon to form a hybrid VDMOSFET-IGBT device. Such a solution as of 2008, the start of the research project, was not yet researched and offered a potential benefit. Such a device would enable single gate control within a relatively rugged DMOS structure of low current density as compared to a trench gate device, albeit on a larger silicon area. Such a hybrid device could also offer benefits in terms of switching frequency and reduced dynamic losses as related to the RC-IGBT type of IGBT devices. The key question would be if the new hybrid would reduce the active area of silicon in relation to an SSPC solution using solely CoolMOS, or MDmesh type SJ MOSFET devices at fault current levels and high temperature. Two parallel projects were therefore begun at the University of Warwick to investigate the hybrid possibility, a vertical structure was called the Hybrid Unipolar-Bipolar Field Effect Transistor (HUBFET) as described by Donnellen[130], which was based on the BiGT device Rahimo[68] and the other laterally injected structure was described and investigated within this work.

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Chapter 3 | Optimisation of VDMOSFET for lowest on state resistance

3.0 Introduction

For use in the More Electric Aircraft (MEA) to enable rugged, remotely placed, long life switching elements of potentially high fault currents, the design aim of this research work was to provide an injected (hybrid) VDMOSFET (Vertical Double diffused Metal Oxide Field Effect Transistor). The injected structure was intended to provide a self biased transition from unipolar to bipolar conduction in that event of a short circuit load fault such that the device would conduct safely a large magnitude transient fault current and perform a repeatable hard switching operation in response to turn off an inductive load. The device was required to have a single voltage controlled gate and achieve lowest static conduction losses during all conditions (both for a nominal and fault current) and achieve the lowest dynamic loss during all switching operations, but particularly turn off. The switching element must also be either free from latch up, or proven to latch up well beyond the expected fault current density level, even at high ambient heat sink temperature (400 K). Such a switching device was targeted for use within a Solid State Power controller (SSPC) for which the device was to be fabricated in silicon (Si).

The decision within chapter 2 was to utilise the DMOS (Double diffused Metal Oxide Semiconductor) gate structure as the basis for the injected hybrid, due to proven ruggedness when used to form either a MOSFET or NPT IGBT (Non Punch Through

Insulated Gate Bipolar Transistor). The device was to be optimised for lowest total on state resistance, $R_{(ON)}$ under all voltage conditions in order to minimise conduction losses. The DMOS, due to it not being active area optimum, would not provide optimum specific on state resistance (where $R_{(ON,SP)} = R_{(ON)} * \text{Area}$), but did however provide a relatively low current density in comparison to a UMOS (Trench gate MOSFET) type construction. The self heating of the device due to high current density through a given resistance (particularly under the gate electrode near the channel) therefore would be less in the event of fault current and hence provided increased ruggedness, but at the cost of increased area. In addition the DMOS structure could also be more versatile than the UMOS as the channel was formed laterally, not vertically thus allowing the channel to be as effective with a lateral anode (placed adjacent to the channel) as it was with an IGBT like vertical anode (placed at the bottom of the wafer).

The aim of this chapter is to optimise the VDMOSFET to ensure lowest static conduction loss via reduction of the total on state resistance (R_{ON}) and yet provide a low threshold voltage ($V_{TH} \approx 5 \text{ V}$), highest possible transconductance in the linear region (g_{mL}) and the highest sub threshold swing (highest dI_A/dV_{GK} , for $V_{GK} < V_{TH}$). The Chapter will first describe the design goal and review the elements of resistance within a VDMOSFET structure. An explanation will then be provided of the basic process flow to create a VDMOSFET and the key parameters to be included within a Design Of Experiment (DOE, using Taguchi statistical optimisation methods). Any improvements to the basic design after the optimisation experiment will then be discussed and a field relief structure will be presented. Finally the resultant VDMOSFET will be compared to those in literature and to the one dimensional (1-D) theoretical silicon limit for unipolar conduction devices, plotted in terms of $R_{(ON,SP)}$ versus Blocking Voltage (BV).

3.1 Design goal of the VDMOSFET

The original requirement for the switching device within the MEA was $BV=500$ V minimum, as specified via the U.S. Military aircraft development programs that required adherence to MIL-STD-704-F [1]. The drift length (D_L) necessary for a 500 V device was dictated by the drift region doping and the resultant extent of the depletion region as discussed later. Of the two types of injected structures (vertical and lateral injector types) then both the vertically injected structure and lateral injected structure would have unique issues in reaching the minimum voltage requirement. For example, the vertical structure recommended in chapter 2 was the NPT-IGBT however, when fabricated in thinned bulk silicon utilising a backside wafer acceptor impurity implant to form the P-Anode as described by Laska[2] at 600 V (100 μm thick), then the thinning operation and subsequent bow management became most difficult to achieve. However, NPT-IGBT designs down to 400 V (40 μm thick) have recently been demonstrated by Boving[3] these had an improved on state voltage drop (V_{AK})/turn off energy (E_{off}) compromise over thicker 600 V devices. The form and optimisation of the implanted vertically placed P-Anode design was one of the subjects of the research work.

The lateral hybrid structure however, was a little more difficult to predict in terms of behaviour and characteristics due to the required proximity of the lateral injector to the channel. The injector needed to be close enough to begin injection of minority carriers (holes) and have low on state voltage (V_{AK}), but this may be in a compromise with the extent of the depletion from the P-body to N-Drift junction. It was therefore decided to start with a fairly low voltage rated VDMOSFET model which could be characterised in both vertical and lateral injected formats in order to understand how the injectors functioned, in particular how the P-Anode to N-Drift junction became forward biased and maintained that bias level. The BV rating could subsequently be increased via ‘standard techniques’, once the dependencies in both lateral and vertical injected devices were fully established. ‘Standard techniques’ included the use of charge balance techniques as described by Fujihira[4] and

Deboy[5], wherein a lower drift length (D_L) was required to enclose $W_{D\text{MAX}}$ and a higher donor doped N-Drift region doping could be used.

A full summary of the general design aims of the proof of injected hybrid concept VDMOSFET are shown in ranked priority order in table 3.1.

Priority rank	MOSFET characteristic	Desired level
1	Blocking Voltage (BV)	≈ 100 V
2	On state resistance ($R_{(ON)}$)	Lowest possible
3	Sub threshold leakage current (blocking mode) (J_L)	Lowest possible
4	Saturation current ($I_{A,sat}$)	Highest possible
5	Transconductance in linear region (g_{mL}), ($V_{AK} = \text{constant}$)	Highest possible
6	Threshold Voltage (V_{TH})	Lowest possible

Table 3.1. General design aims of the MOSFET to form the basis of the injected hybrid.

3.2 Contributory elements of VDMOSFET total resistance

The contributory factors to the total on state resistance of the VDMOSFET are indicated in relation to the VDMOSFET structure as shown in figure 3.1 a). The relative

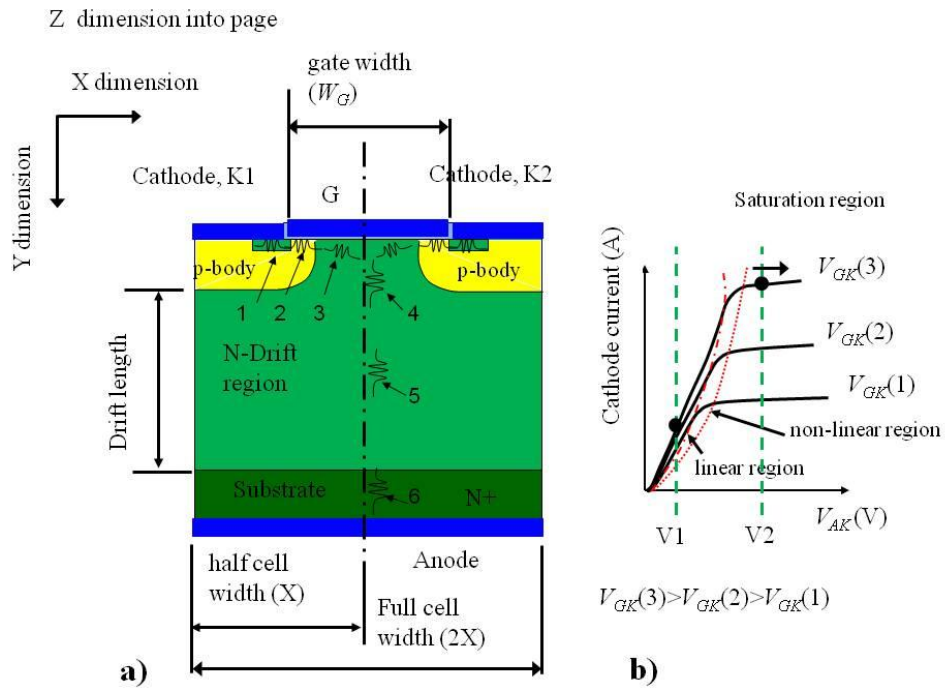


Figure 3.1. VDMOSFET cell showing a) Elements of resistance b) generalised forward conduction characteristic at ambient heat sink temperature (T) =300 K.

magnitude of each resistive element identified, as a contributory factor to the total on state resistance, is also varied as a function of terminal bias (anode to cathode voltage (V_{AK}),

assuming $V_{GK} \gg V_{TH}$) as indicated by comparison of table 3.2 with the generic forward I-V characteristic shown in figure 3.1 b).

Approximated percentage contribution	N+ cathode (1)	Channel (2)	Accumulation (3)	JFET (4)	Drift (5)	Substrate (6)
At V1 (fig 3.1b)	0.4	25	16	8	48	2.6
At V2 (fig 3.1b)	0.1	80	2	1.5	16	0.4

Table 3.2. Variation of resistance contribution with increasing terminal voltage (V_{AK}) for a $BV=100$ V VDMOSFET design (using figure 3.1 b).

The factors influencing the total on state resistance, $R_{(ON)}$ of the VDMOSFET are well understood and described by Baliga[6]. There follows a brief description of each of the major resistive elements.

3.2.1 Drift resistance

The influence of and resulting percentage contribution of the drift region resistance (5) to the total $R_{(ON)}$ is directly influenced by the blocking voltage (BV) requirement and selected drift region donor doping concentration (N_d). The BV for the one sided step junction where acceptor doping in the P-body is at least one order of magnitude greater than the donor doping of the drift region is as follows:-

$$BV = \frac{\epsilon_{\max} W_{DMAX}}{2} = \frac{K_s \epsilon_o \epsilon_{crit}^2}{2qN_d} \text{ (V)} \quad (3.1)$$

$$W_{DMAX} = \left(\frac{2K_s \epsilon_o V_{AK}}{qN_d} \right)^{0.5} \text{ (cm)} \quad (3.2)$$

Equations 3.1 and 3.2 are solutions of the one dimensional (1-D) Poisson's equation related to the abrupt P-N junction as shown in equation 3.3 and shown in figure 3.2. According to Baliga[6], equation 3.3 describes the charge in the donor doped side of a P-N junction, in this case the P-body to N-Drift junction. The electric field and voltage at any point along the X dimension can be calculated using equations 3.4 and 3.5 respectively, shown in figure 3.2.

$$\frac{d^2V}{dX^2} = -\frac{d\epsilon}{dX} = -\frac{Q(X)}{K_s \epsilon_o} = -\frac{qN_d}{K_s \epsilon_o} \quad (3.3)$$

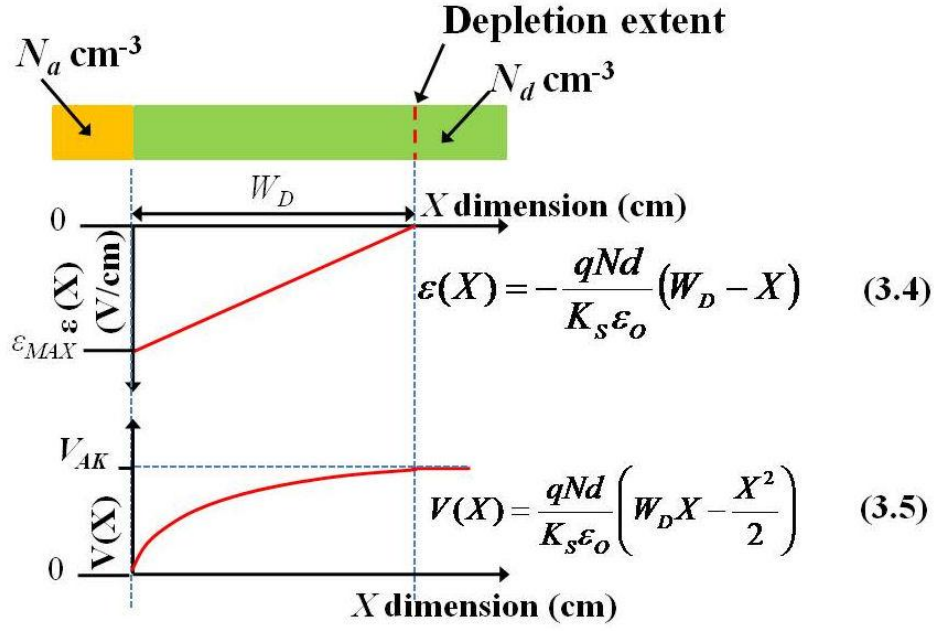


Figure 3.2. Electric field and potential distribution for an abrupt parallel-plane P-N junction, ($N_a > N_d$ by at least one order of magnitude). Baliga[6].

Obviously from equation 3.1 an increased level of impurity doping concentration (N_d), will result in a lower BV , but as regards the maximum depletion width, $W_{D_{MAX}}$, as given by equation 3.2 then an increase in N_d would result in a reduction in the depletion extent from the P-body into the N-Drift region. Ideally in a VDMOSFET design the $W_{D_{MAX}}$ should not be allowed to reach the substrate or punch-through may occur in to the low N_a doped channel region and the N+ source to P-body depletion may touch the P-body to N-Drift depletion which in effect short circuits the cathode and anode. The drift length therefore is dependent upon the drift region doping concentration (N_d), whereas the drift region resistance (5 in table 3.1) is dependant both upon the drift length and the doping concentration as shown in equations 3.6 and 3.7.

$$R = \rho \frac{L}{A} (\Omega) \quad (3.6)$$

$$\text{Where: } \rho = \frac{1}{q\mu_n N_d} (\Omega\text{cm}) \quad (3.7)$$

L = Drift length, A = cross sectional area of drift region ($A = X * Z$ dimensions)

The electron mobility (μ_n) used in equation 3.7 also changes with donor concentration as shown in figure 3.3 a). At a given donor concentration the mobility also changes with lattice

temperature as shown in figure 3.3 b). Thus, with increasing lattice temperature the resistance of the VDMOSFET increases with temperature (positive temperature coefficient).

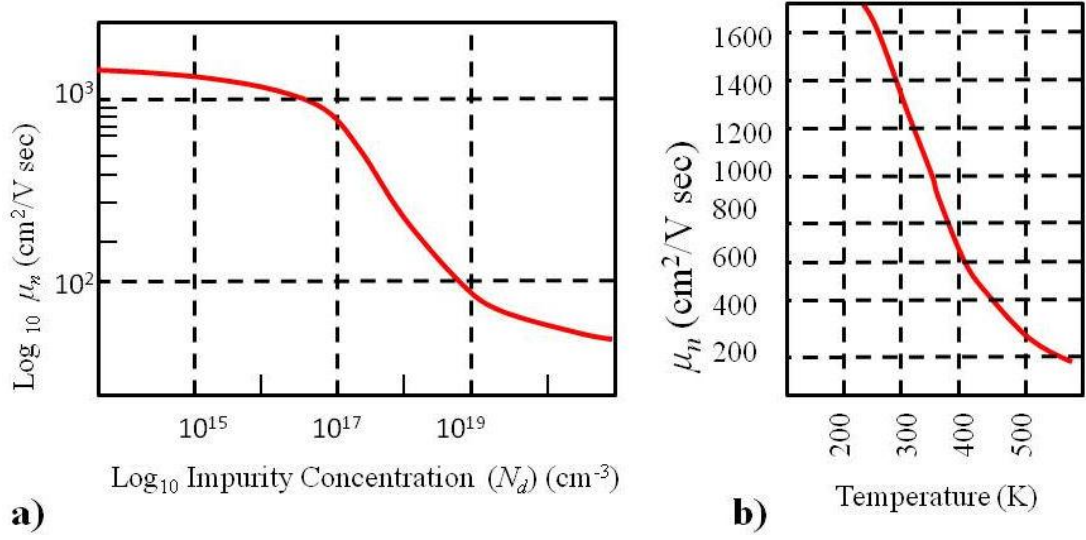


Figure 3.3. Electron Mobility (μ_n) variation with a) concentration, b) temperature. Baliga[6].

The term “one dimensional silicon limit” (1-D silicon limit) was an expression derived from the inverse relationship between BV and drift region concentration (N_d) within unipolar semiconductor devices. The aim in every semiconductor device is to minimise on state loss through a reduction of resistivity, thus requiring a high N_d , but this caused a reduction in BV . The work of Hu[7] provided an expression in terms of ($R_{(ON,SP)}$ and BV) to describe the 1-D or doping interdependence between the dependant drift resistance to and BV level, this subsequently became known as the “1-D silicon limit” for n-type drift regions as shown in equation 3.8. Due to the reduction in mobility within p-type drift regions, the calculated magnitude of $R_{(ON,SP)}$ must be multiplied by a factor of 2.5, according to Hu[7]. The one dimensional aspect meant that the calculation was based on doping only, where for example the BV calculation did not include 2-D effects such as the P-body radius effects etc.

$$R_{(ON,SP)} = 3.7E - 9(BV)^{2.6} \text{ (}\Omega\text{cm}^2\text{)} \quad (3.8)$$

3.2.2 Effect of cell width on JFET and drift resistance

The other major factor affecting the $R_{(ON)}$ of a unipolar power device is cell width as described by Baliga[6]. The optimum cell width occurs when the electron ‘funnel’ from the substrate to the channel is contained exactly by the cell dimensions as shown in figure 3.4a. The angle of 45° remains constant, but if the drift length is reduced for the same cell width, as in figure 3.4b, then the design would be wasteful on unused conduction area. Whilst the other extreme, when the drift length was increased (as shown in figure 3.4c), then the $R_{(ON)}$ was also increased due to the reduced effective anode area available to the cell. The ratio of drift length to cell width is therefore important to minimising the on state resistance, $R_{(ON)}$. However, the minimum cell width according to Baliga[6] is constrained both by the design rules (which determine the minimum feature size) and by the neck width of the “funnel” at a given operational forward voltage due to impingement of the adjacent P-body to N-Drift depletion regions. If the gate width (W_G) is made larger, this then results in the funnel ‘neck’

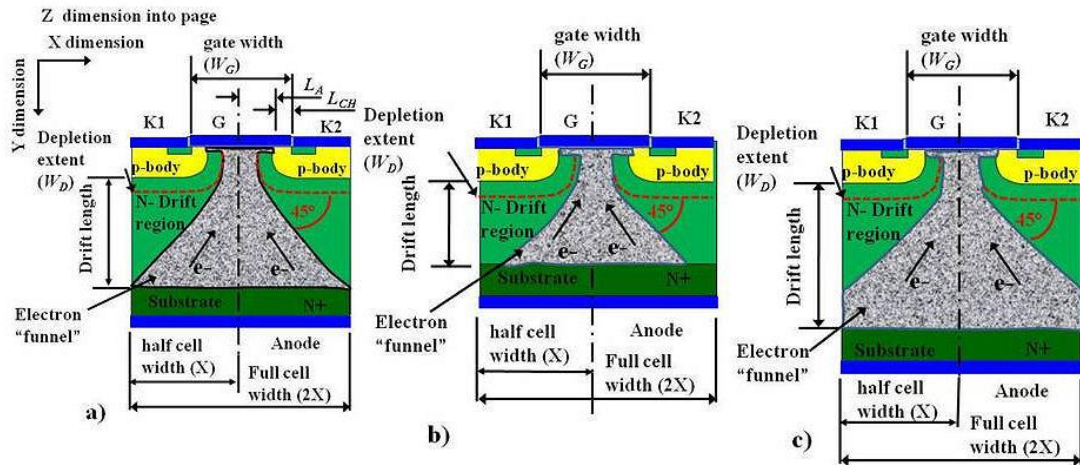


Figure 3.4. Effect of cell dimensions on the on state resistance, $R_{(ON)}$, of a VDMOSFET, gate width (W_G) held constant.

dimension also increasing thus, reducing the JFET resistance (resistor 4, in figure 3.1). If the drift length is kept larger than necessary for the required BV , then the drift length could be subsequently reduced following gate width optimisation. Thus, the cell width to drift length ratio could be optimised to achieve lowest on state resistance, $R_{(ON)}$, for an optimum active area (A). The effect of gate width on the JFET resistance can be seen in figure 3.5.

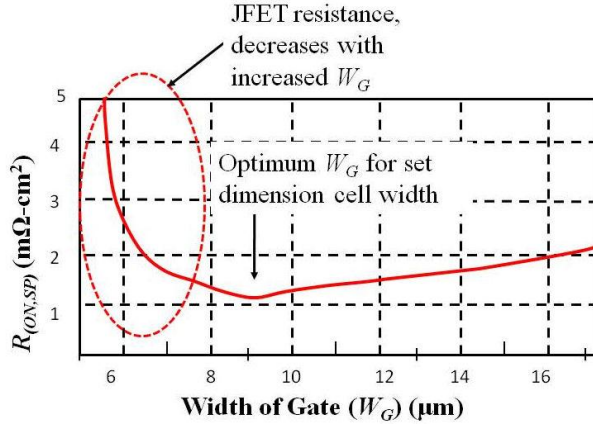


Figure 3.5. Effect of gate width (W_G) on $R_{(ON,SP)}$ to find optimum dimension of W_G .

3.2.3 Channel and accumulation region resistance

As regards the proportionate contribution of each factor, as shown in table 3.1, then when operating within the linear region the on state resistance, $R_{(ON)}$, is maintained approximately constant, therefore the forward current is linearly dependent upon the forward voltage dictated by the factor $R_{(ON)}$. As terminal bias is increased (at a given level of V_{GK}), then at low current and voltage (V1, as shown in figure 3.1 b) the drift resistance is the major contributory factor, followed by the channel and accumulation regions due to the increased carrier concentration in those areas which caused a reduction local mobility and hence increased the resistance in those areas. This assumes that the channel is fully inverted and the terminal bias increases with current in the linear region.

Similar to the drift resistance the channel resistance is a function of the channel length (L_{CH}), as stated earlier the channel, when inverted, consist of a high concentration of electrons where $N_d \approx 1E19 \text{ cm}^{-3}$ (which are classed as minority carriers within the acceptor doped P-body) and subsequently has an inversion layer mobility (μ_{ni}) which would be much less than the μ_n achieved in the N-Drift region as demonstrated in figure 3.3 a. The channel resistance was expressed by Baliga[6] as shown in equation 3.9. Obviously, from equation 3.9 a reduction in L_{CH} causes a reduction in the channel resistance.

$$R_{CH} = \frac{L_{CH}}{Z\mu_{ni}C_{OX}(V_{GK} - V_{TH})} \text{ (}\Omega\text{)} \quad (3.9)$$

Where $L_{CH} = Y_{JP} - Y_{N+}$ (assuming lateral rotation of the Y dimension acceptor doping profile of the P-body). The accumulation resistance (R_A) is calculated as per equation 3.9, but substituting the dimension L_A for L_{CH} . Where the dimensions L_A and L_{CH} are shown in figure 3.4 a).

Entry into the non linear region of the characteristic as shown in figure 3.1b) is an indicator that the channel is about to be pinched off should the current continue to rise thereby having an increased effect in raising the voltage (V_{AK}). This is caused by the voltage developed in the acceptor doped P-body along the length of the inverted channel due to the electron flow. Eventually the developed voltage is large enough to counteract the gate voltage (V_{GK}) which subsequently reduces the effective gate bias to reduce the threshold voltage, thus the inversion layer is lost at the anode side of the channel where the acceptor doping is lowest and represents the point of the lowest threshold voltage level along the length of the channel as described by Greve[8]. At V_2 of figure 3.1 b) therefore, the VDMOSFET has entered saturation and the channel is pinched off, thereafter any increase in current is due purely to channel length modulation as described by Yang[9], Sze[10] and Grove[11]. Entry in to the saturation state was to be avoided because the active area of the VDMOSFET was fixed, therefore if more current was required by a load fault beyond the total saturation current density level ($J_{A,sat}$) then the terminal bias would quickly rise and may cause avalanche and ultimately thermal failure of the device.

3.2.4 Other resistances

The other resistances include the N+ cathode resistance and the substrate resistance both are calculated as per the drift region resistance and the respective lengths are required to be kept as short as possible. In particular it is desired to keep the N+ cathode to be extremely short as this is a technique to increase the hole current required through the P-body to cause bipolar activation of the parasitic NPN Bipolar Junction Transistor (BJT) reported to cause latch up in IGBT type of MOS controlled devices.

The effect of the substrate resistance, if reviewed in terms of the active cell area, can be large when considered relative to the drift length, especially in low voltage MOSFET designs with relatively small drift length. For example equation 3.11 shows the resistance of a typical substrate thickness of $L_{Sub}=300 \mu\text{m}$, doped to $N_d = 1\text{E}19 \text{ cm}^{-3}$. Whereas the benefits of a reduced thickness substrate to $L_{Sub}=120 \mu\text{m}$, also doped to $N_d = 1\text{E}19 \text{ cm}^{-3}$ can be seen in equation 3.12, (assuming a cell active area, $A= 1\text{E}-4 * 11\text{E}-4 \text{ cm}^2$). As can be seen a reduction in substrate thickness, even at high doping concentrations can provide a substantial reduction in the resistance associated with the substrate.

$$R_{Sub} = \left(\frac{L_{Sub}}{A} \right) \left(\frac{1}{q\mu_n N_d} \right) \quad (3.10)$$

$$R_{Sub} = \left(\frac{300\text{E}-4}{0.11\text{E}-6} \right) \left(\frac{1}{1.6\text{E}-19 * 1350 * 1\text{E}19} \right) = 1.26\text{E}20 (\Omega) \quad (3.11)$$

$$R_{Sub} = \left(\frac{120\text{E}-4}{0.11\text{E}-6} \right) \left(\frac{1}{1.6\text{E}-19 * 1350 * 1\text{E}19} \right) = 235.6\text{E}6 (\Omega) \quad (3.12)$$

3.3 The MOS capacitor and effect on VDMOSFET performance

The operation of the MOS capacitor formed in silicon and the effects of that on the threshold voltage (V_{TH}), anode current (I_{AK}), saturation current ($I_{A,sat}$) and transconductance in the linear region (g_{mL}) are well researched and documented. A summary was provided by Baliga[6] for a direct understanding of VDMOSFET operation. Important formulas to this design are as follows in equations 3.13 to 3.18 inclusive, as derived by Baliga[6].

$$V_{TH} = \frac{\sqrt{2K_s \epsilon_o q N_a 2\psi_B}}{C_{OX}} + 2\psi_B \text{ (V)} \quad (3.13)$$

$$I_K = \frac{Z\mu_{ni}C_{OX}}{2L_{CH}} \left[2(V_{GK} - V_{TH})V_{AK} - V_{AK}^2 \right] \text{ (A)} \quad (3.14)$$

$$I_{A,sat} = \frac{Z\mu_{ni}C_{OX}}{2L_{eff}} (V_{GK} - V_{TH})^2 \text{ (A)} \quad (3.15)$$

$$g_{mL} = \frac{dI_K}{dV_{GK}} = \frac{Z\mu_{ni}C_{OX}}{2L_{CH}}V_{AK} \text{ (S)} \quad (3.16)$$

$$C_{OX} = \frac{K_O\epsilon_O}{t_{OX}} \text{ (F)} \quad (3.17)$$

$$\psi_B = \left(\frac{E_i - E_{FS}}{q} \right) = \frac{kT}{q} \ln \left(\frac{N_a}{n_i} \right) \text{ (V)} \quad (3.18)$$

An obvious course of action to decrease V_{TH} , increase $I_{A,sat}$ and transconductance (g_{mL}) is to increase C_{OX} via a reduction in t_{OX} however, there is a minimum limit on the oxide thickness due to dielectric breakdown of the oxide (which is approximately 1×10^7 V/cm). Unfortunately, this is further complicated by edge effects where high electric fields occur at the gate electrode edge as described by Sze[10]. Such edge effects can be minimised by running the gate electrode contact material (N+ polysilicon or aluminium) over the field oxide, thus reducing the corner radius.

In the absence of further reduction in t_{OX} then to reduce V_{TH} the P-body acceptor doping can be minimised as indicated in equation 3.10. However, if N_a was made too low then punch through of the P-body would occur as shown in figure 3.6. Punch through would also occur at relatively low V_{AK} magnitudes if L_{CH} was made too short. The sub-threshold current of a VDMOSFET according to Sze[10] is ideally extremely low when $V_{GK} < V_{TH}$ even if V_{AK} is increased, however it is required to rise extremely rapidly in the event that V_{GK} approaches V_{TH} . The requirements for such a sub threshold current according to Sze are a low channel doping (N_a) and a thin gate oxide (t_{OX}), however, if N_a is too low then sub threshold current will rise due to punch through effects as described above.

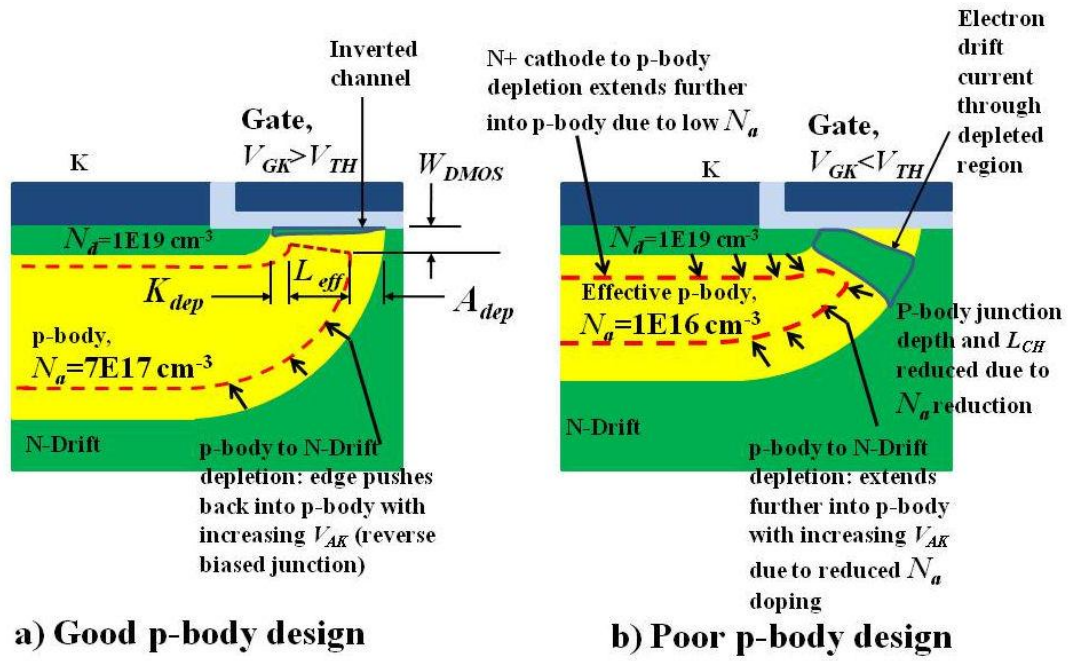


Figure 3.6. Punch through caused by low acceptor doping of the P-body causing short circuit of the cathode to anode.

On inspection of equations 3.13 for V_{TH} and 3.18 for ψ_B the threshold voltage has a dependence on lattice temperature; the effect is that V_{TH} will reduce with increased temperature. Therefore the V_{TH} level must be set so that the device does not become ‘normally on’ at high lattice temperature, or suffer high sub threshold (leakage) current. According to Sze[10] the oxide thickness and P-body acceptor doping need to be minimised to decrease the rate of change in V_{TH} as temperature rises.

3.4 VDMOSFET basic process flow

The basic VDMOSFET process flow as shown in figure 3.7 was used as a basis for the design optimisation. This multi masked process required that the gate oxide be deposited first to ensure the cleanest (charge free) oxide interface to the epitaxial silicon layer. A CVD deposited poly silicon layer then forms the gate electrode. The subsequent oxide deposition and definition of the gate electrode via photolithographic step then provides the ion implant mask for the P-body and N+ source as described by Yoo[12]. In this sequence the P+ cathode short is ignored, but the general principle of incorporating impurities into the silicon

lattice is otherwise identical, forming a repetitive cycle of growing or depositing an oxide, opening a window in the oxide via photolithography, then implanting and thermal annealing the diffuse and activate it within the lattice. The use of Antimony (Sb) in the substrate helps prevent auto doping of the grown epitaxial drift layer as the element is large and heavy therefore has minimised thermal diffusion.

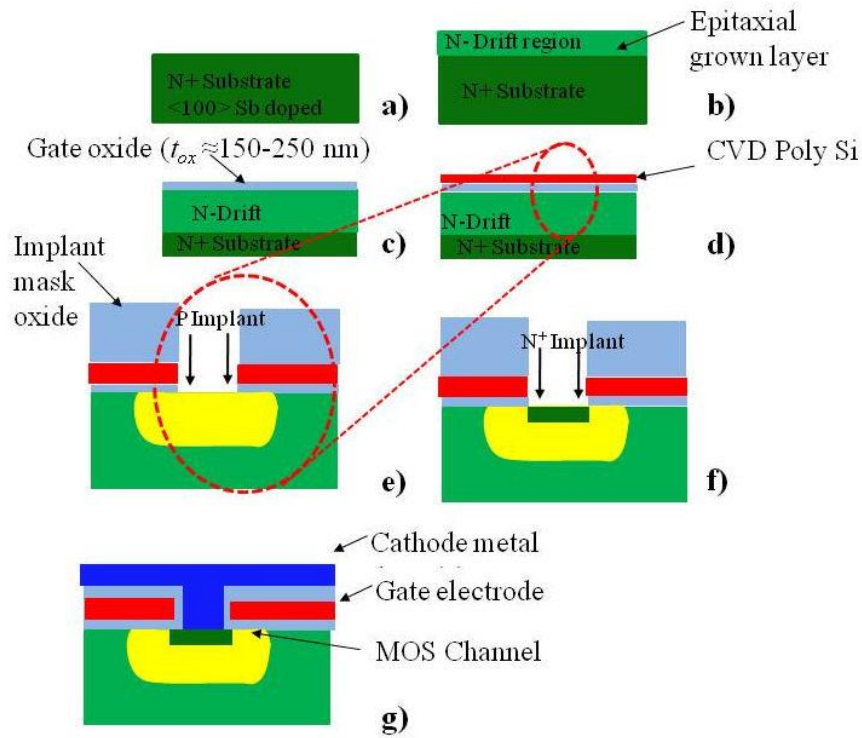


Figure 3.7. Basic self aligned VDMOSFET process flow.

It is essential to obtain the best interface possible between the gate oxide and the silicon to obtain the highest channel mobility. Figure 3.8 shows the MOS capacitor interface structure as along with the fixed charges, mobile ion charge (typically, Q_{Na^+}) and interface charges as described by Baliga[6]. These trapped charges have the effect of negatively adjusting V_{TH} from the theoretical value due to the resultant energy band bending. Such charges can be minimised by growing the gate oxide first which remains in place throughout the remainder of the processing. According to Baliga[6] the impact of a positive fixed charge (assumed to be at the metal to oxide interface) due to the total effective charge in the oxide

(Q_{OX}) can be calculated using equation 3.19. With the use of the $\langle 100 \rangle$ crystal orientation surface of silicon then the interface charges can potentially be reduced to around ($2 \times 10^{10} \text{ cm}^{-2}$) with effective process control according to Baliga[6]. The MOS depletion extent due to the electric field perpendicular to the silicon surface when $V_{GK} > V_{TH}$ is also shown in figure 3.8.

$$V_{TH} = \frac{\sqrt{2K_s \epsilon_o q N_a 2\psi_B}}{C_{OX}} + 2\psi_B - \frac{Q_{OX}}{C_{OX}} \quad (\text{V}) \quad (3.19)$$

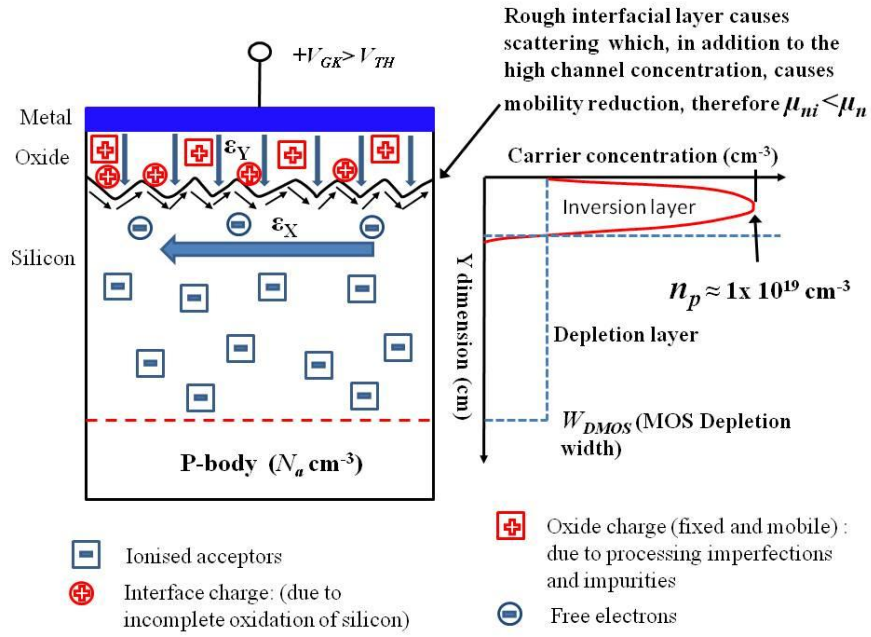


Figure 3.8. Oxide to silicon interface showing the electric field relationship, trapped charges (which affect V_{TH}), and the effects on channel mobility. Baliga[6].

In order to obtain the correct doping profiles within the structure programmed into the Synopsys Medici simulator[13] then in addition to a definition statement as to the location and size of the oxide window, in this work a Gaussian doping profile was utilised. To define the Gaussian profile a peak doping concentration was declared together with the Y dimension at which that the peak concentration occurred at. A characteristic length was then provided to set the spread (or range), alternatively the metallurgical junction depth could be declared which enabled Medici to calculate the required range within the N-Drift doping. A lateral rotation was then used as an estimate as to the lateral spread of the diffused impurity

atoms under the adjacent oxide layers left by the masked lithography stage. An example of the doping and diffusion process is shown in figure 3.9.

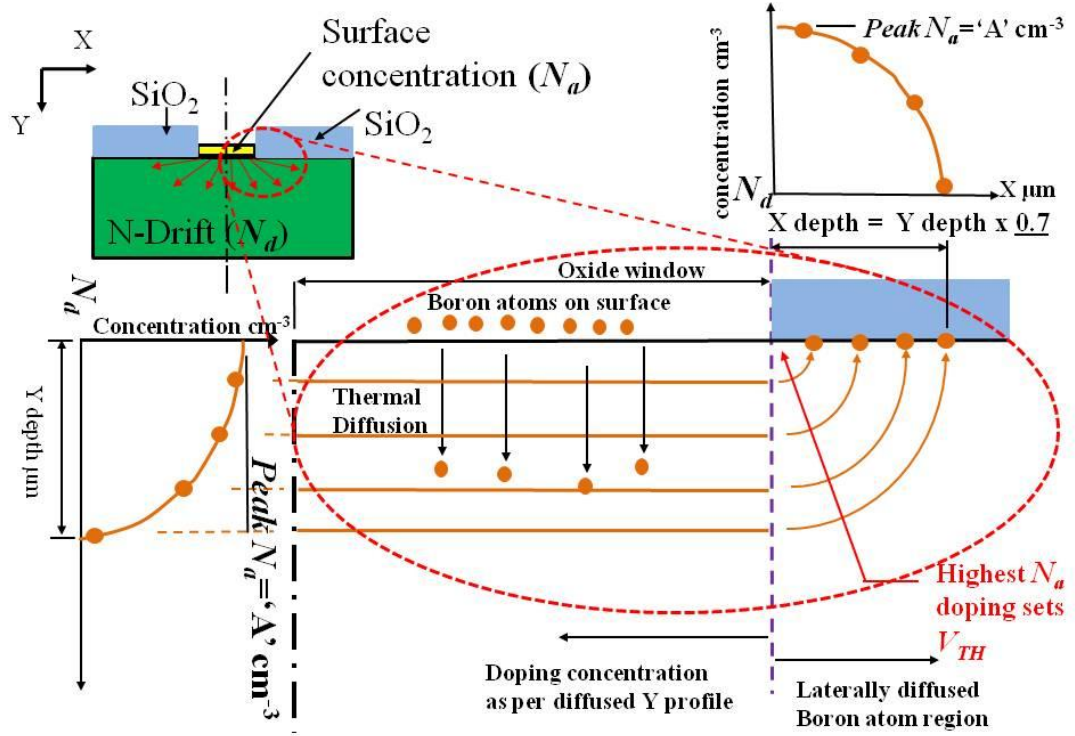


Figure 3.9. Use of rotational factor to obtain lateral (X) diffusion profile from vertical (Y) profile. Rotational factor = 0.7, assumes no out diffusion in to SiO₂.

3.5 Summary of important half cell design parameters

The aim of this section is to summarise the theory that affects the forward static conduction performance of the VDMOSFET in terms of the design goals described within table 3.1.

Using the theory described in sections 3.2 and 3.3 a list of processing factors relevant to the design aims as stated in table 3.1 is summarised in table 3.3.

The depletion capacitance (C_d) was included in table 3.3 as that has a direct influence on the dynamic losses of the VDMOSFET due to the time required to charge the gate capacitance at turn on and discharge the capacitance at turn off as described in relation to an IGBT by Chokhawala[14, 15]. The depletion capacitance (C_d) due to the depletion extent into the acceptor doped channel region to a depth of (W_{DMOS}) is added in series to the MOS capacitance (C_{OX}) to form the total gate capacitance (C_{TOT}) as shown in equation 3.21.

Processing Factor	Aspect of VDMOSFET performance affected by given processing factor
Acceptor doping of P-body (N_a)	<ol style="list-style-type: none"> 1) V_{TH} 2) Sub threshold current 3) I_A & $I_{A,sat}$ 4) Transconductance (g_{mL}) 5) Depletion capacitance (C_d) and maximum width (W_{DMOS}) 6) Inversion layer effective mobility 7) Threshold voltage shift with temperature 8) BV (both 1-D and due to 2-D radius effects)
Gate oxide thickness (t_{OX})	<ol style="list-style-type: none"> 1) Sub threshold current (via μ_{ni} effects due to charge) 2) V_{TH} 3) MOS capacitor breakdown 4) I_A & $I_{A,sat}$ 5) Transconductance (g_{mL}) 6) Depletion capacitance (C_d) and maximum width (W_{DMOS}) 7) Threshold voltage shift with temperature
P-body junction depth	<ol style="list-style-type: none"> 1) Channel resistance (via channel length L_{CH}) 2) I_A & $I_{A,sat}$ 3) Transconductance (g_{mL})
N+ cathode junction depth	<ol style="list-style-type: none"> 1) Channel resistance (via channel length L_{CH}) 2) I_A & $I_{A,sat}$ 3) Transconductance (g_{mL})
Half cell width	<ol style="list-style-type: none"> 1) JFET resistance reduction 2) Optimisation of gate width/cell width and drift length 3) BV (via adjacent P-body shielding effect)
Gate to cathode gap	<ol style="list-style-type: none"> 1) Gap required to be short as possible to reduce N+ cathode resistance.
N-Drift doping concentration	<ol style="list-style-type: none"> 1) BV of device as supported by P-body to N-Drift junction 2) Resistivity of N-Drift region length

Table 3.3. Summary of the effect of key process factors on a VDMOSFET design performance.

$$C_d = \frac{K_o \epsilon_o}{W_{DMOS}} \text{ (F)} \quad (3.20)$$

$$C_{TOT} = \frac{C_{OX} C_d}{C_{OX} + C_d} = \frac{1}{\frac{C_{OX}}{C_d} + 1} \text{ (F)} \quad (3.21)$$

With use of table 3.3 a summary of the variables to be included in the design of experiment (DOE) to optimise the design for lowest on state loss can be provided in the form of a diagram of the P-body and channel as shown in figure 3.10.

As shown in figures 3.9 and 3.10 the peak doping concentration during the DOE was declared at the surface of the silicon, a Gaussian profile to the required metallurgical junction depth was then calculated by Synopsys Medici[13]. The lateral rotation factor as shown in figure 3.9 was 0.7, hence the dimension L_{CH} was determined by the P-body junction depth, the continuously refreshed peak surface concentration and the Synopsys calculated Gaussian doping profile in the Y dimension. The oxide window dimensions for both the P-body diffusion and the N+ cathode diffusion were fixed, as detailed in figure 3.11

together with other fixed control factors of the DOE. The basic VDMOSFET design used for the DOE did not incorporate a self aligned gate and assumed an additional mask stage to set the gate width and gate to cathode oxide gap.

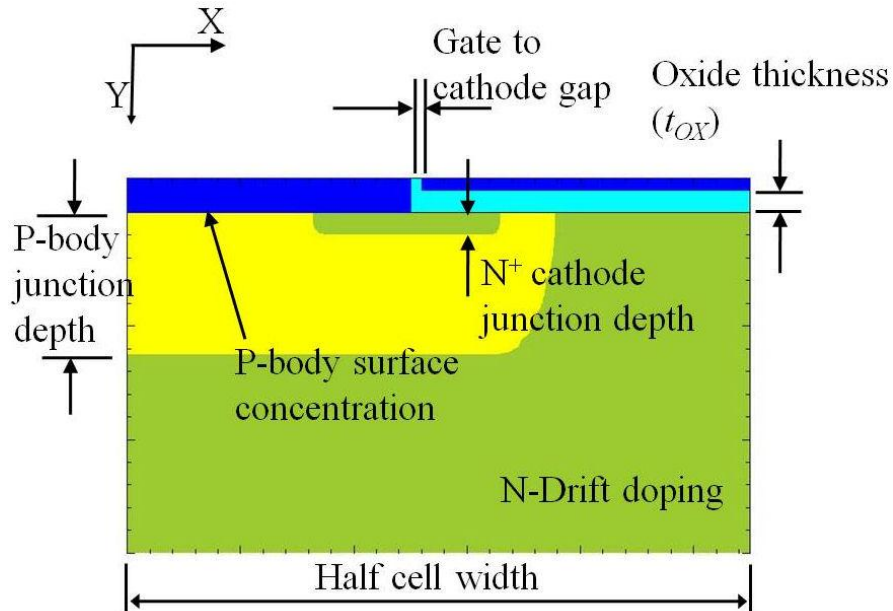


Figure 3.10. The varied control factors to be used within the design of experiment (DOE) to optimise the VMOSFET design for lowest on state loss.

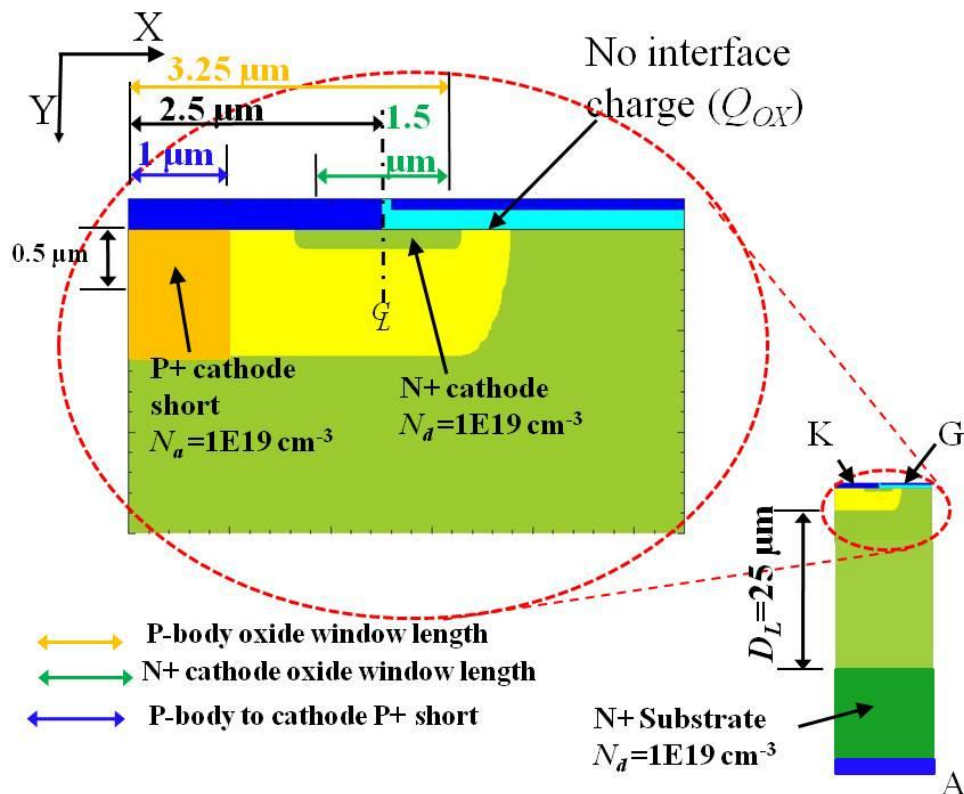


Figure 3.11. Diagram showing the fixed control factors used during the DOE.

3.6 Design of experiment (half cell optimisation)

The statistical method for the design of experiment work was devised by G. Taguchi[16, 17], originally the method was developed to provide robust process parameter designs that would provide high quality, repeatable workmanship despite the influence of “noise factors” such as variation in gas pressure, or variation in temperature for example within a furnace. Such applications of the method were discussed by Taguchi[18] and Byrne[19], however the DOE method developed could also be used to design product, again, to provide optimum repeatable performance, Taguchi[20]. Essentially the systematic method developed replaced the traditional random adjustment of one factor at a time in order to resolve a given issue; instead the system took all the known control parameters and assessed the inevitable interactions between them, resulting in a setting on each to provide an optimum design which was robust to slight variation in any single or multiple parameters. The method has found wide acceptance and use within industry, but its use was the subject of academic debate, as described by Nair[21].

3.6.1 Selection of DOE array and control variable levels

Taguchi developed and then defined through calculation a number of orthogonal arrays for use by practitioners of the method. For example practitioners seeking to use parameter design techniques to obtain a design which is robust to potential causes of variation, such as those related to manufacturing control parameters. Equally the technique can be applied to parameters known to affect design performance. The selection of which array to use is critical to the experimental time and success. The selection of the orthogonal array is dependent upon the number of control factor variables (design parameter variables) and the maximum number of setting levels for each variable. In this DOE the number of control factors was 7, utilising 3 level settings for each in order to indicate a trend. An orthogonal array selection tool such as provided by Free quality[22] advised the use of an L18 array as shown in table 3.4. The Array was used to dictate the number of trials and the selection of level settings for each trail, in this case 18 trials were utilised. As the L18 provisioned for 8

control variables one column was left idle, as described by Grove[23], (in this case column 1 was left idle, as shown in red).

The level settings for the DOE were as shown in table 3.5, these values were selected using the information provided in the preceding sections to provide a reasonable range of settings which would indicate a trend.

Trial No	Column							
	1	2	3	4	5	6	7	8
1	1	1	1	1	1	1	1	1
2	1	1	2	2	2	2	2	2
3	1	1	3	3	3	3	3	3
4	1	2	1	1	2	2	3	3
5	1	2	2	2	3	3	1	1
6	1	2	3	3	1	1	2	2
7	1	3	1	2	1	3	2	3
8	1	3	2	3	2	1	3	1
9	1	3	3	1	3	2	1	2
10	2	1	1	3	3	2	2	1
11	2	1	2	1	1	3	3	2
12	2	1	3	2	2	1	1	3
13	2	2	1	2	3	1	3	2
14	2	2	2	3	1	2	1	3
15	2	2	3	1	2	3	2	1
16	2	3	1	3	2	3	1	2
17	2	3	2	1	3	1	2	3
18	2	3	3	2	1	2	3	1

Table 3.4. L18 orthogonal array used for the DOE.

Column	Control factor	Units	Level 1	Level 2	Level 3
2	Half cell width	μm	4.5	5	5.5
3	N-Drift concentration (N_d)	cm^{-3}	6E14	1E15	3E15
4	P-body junction depth	μm	1.25	1.5	1.75
5	P-body (N_a) surface concentration	cm^{-3}	3E16	3E17	7E17
6	N+ cathode junction depth	μm	0.1	0.2	0.3
7	t_{OX}	μm	0.10	0.20	0.25
8	Gate to cathode gap*	μm	0.05	0.10	0.15

Table 3.5. Variable control factor settings for the DOE.

*Levels chosen of gate to cathode gap were unfeasibly small due to tolerances in photolithography

3.6.2 Experimental method and results

Each trial was completed using the Synopsys Medici simulator[13] (each simulation was programmed using utilising an identical template program for the basic VDMOSFET design, with each incorporating the same set of models and associated programmed control parameters (such as carrier lifetime, τ_N , τ_P) to replicate semiconductor carrier behaviour at an isothermal temperature of 300 K). The trials were conducted in accordance with the L18 orthogonal array, selecting the level setting for each control variable from table 3.5 for each trial number; 1 through 18. For each trial the resulting forward dc characteristics were obtained over a range of gate bias (V_{GK}), from which a transfer characteristic was obtained at $V_{AK}=15\text{ V}$ as shown in figure 3.12, in addition the BV achieved was obtained. The monitored

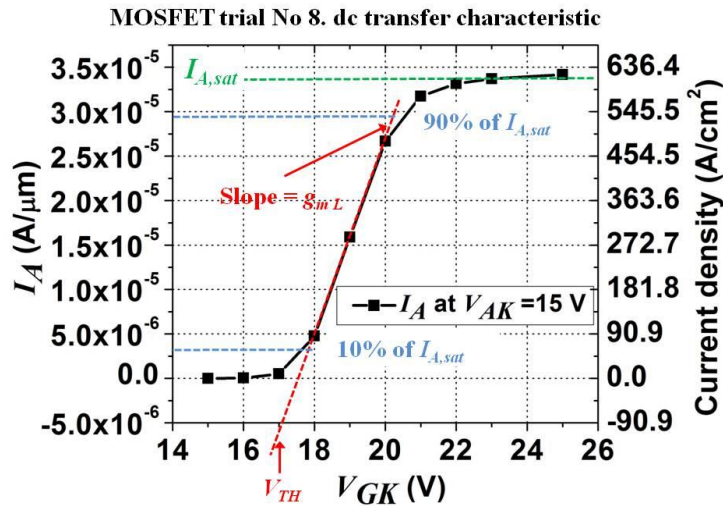


Figure 3.12. Typical dc transfer characteristic showing method of obtaining V_{TH} , g_{mL} and $I_{A,sat}$.

response factors from each trial were: BV , V_{TH} , g_{mL} , $I_{A,sat}$ (at $V_{AK} = 15V$), I_A (at $V_{GK}=0.1V$), I_A (at $V_{GK}<V_{TH}$). The full results for each trial are shown in table 3.6.

Trial No	BV	V_{TH}	$I_{A,sat}$ at $V_{AK}=15$ V	V_{GK} at which $I_{A,sat}$ taken	I_A ($V_{GK}<V_{TH}$)	V_{GK} at which I_A taken	I_A (at $V_{GK}=0.1$ V)	g_{mL}
Units	(V)	(V)	(A/ μ m)	(V)	(A/ μ m)	(V)	(A/ μ m)	(S)
1	38	1	1.42E-05	3	1.30E-11	0.5	5.43E-15	9.62E-06
2	280	13.25	1.39E-05	17	3.23E-09	12	9.65E-16	3.46E-06
3	125	28.75	3.21E-5*	30	8.41E-08	27	9.39E-16	6.4E-6*
4	370	14.5	1.90E-05	21	4.84E-09	13	1.02E-15	3.10E-06
5	265	10.75	2.85E-05	14	4.20E-09	10	1.07E-15	7.11E-06
6	30	2	8.42E-05	10	6.14E-10	1.5	1.31E-15	1.34E-05
7	25	2.25	2.25E-05	6	1.52E-09	1	1.18E-14	4.74E-06
8	270	16.5	3.42E-05	23	2.17E-09	15	1.18E-15	7.81E-06
9	125	11.75	1.22E-04	16	3.08E-09	10	1.14E-15	2.04E-05
10	360	21.75	3.76E-06	26	1.50E-08	21	9.25E-16	7.49E-07
11	10	0.5	2.28E-05	5	9.05E-09	0.1	9.04E-09	6.64E-06
12	120	7.25	5.59E-05	12	3.65E-10	6	9.40E-16	1.78E-05
13	360	26.75	3.21E-5*	30	6.20E-09	24	1.02E-15	1.37E-05*
14	75	1.75	2.62E-05	5	2.19E-12	1	1.70E-15	1.02E-05
15	125	12.3	9.73E-05	20	1.55E-09	11	1.04E-15	1.83E-05
16	350	7	2.00E-05	9.5	5.39E-10	6	1.13E-15	1.27E-05
17	265	21.25	3.89E-05	26	6.22E-08	20	1.18E-15	9.43E-06
18	9	0.5	1.08E-04	10	3.31E-08	0.1	3.31E-08	1.32E-05

Table 3.6. Results of VDMOSFET optimisation DOE. (* indicates full channel inversion of trial structure was not possible within V_{GK} max= 30 V.

3.6.3 Post processing of DOE results data

The results of table 3.6 were statistically processed to obtain the mean response for a given control factor variable at any given level. An example calculation for the mean response to the N-Drift doping control factor as regards BV is shown in table 3.7.

N-Drift doping level	$N_d(\text{cm}^{-3})$								Sum	Mean
1	6.00E+14	Trial No	1	4	7	10	13	16		
		BV obtained	38	370	25	360	360	350	1503	251
2	1.00E+15	Trial No	2	5	8	11	14	17		
		BV obtained	280	265	270	10	75	265	1165	194
3	3.00E+15	Trial No	3	6	9	12	15	18		
		BV obtained	125	30	125	120	125	9	584	89

Table 3.7. Example mean response calculation for BV .

In the example of table 3.7 clearly level 1 provided the highest mean response (251), which is as anticipated from inspection of equation 3.1. Similar calculations were made for each of the varied control factors. For each response factor (BV and anode current, I_A), a plot of the response to each control factor was then made against the same BV scale and anode current (I_A) scale as shown in figures 3.13 and 3.14 respectively. Comparison of the respective plots then enabled selection of the pertinent factors that enabled highest BV , or highest conductivity (or lowest static conduction losses).

To obtain the best compromise, or optimised solution, between the selection of levels to achieve both high BV and high $I_{A,sat}$ simultaneously in the same design, then obviously the inverse relationship as regards the N-Drift doping concentration (column 3) presents the largest issue, choice would depend on priority. In this case from table 3.1 the aim was to provide lowest on state loss in a MOSFET rated to $BV=100\text{-}150\text{ V}$. Thus a compromise on N-Drift doping was clearly required. Support to achieve an increased BV , if

a high N-Drift doping was chosen, was available from column 5 the P-body surface concentration, however a high P-body surface concentration would result in a high V_{TH} , thus restraint was required in terms of N_a . For the factors with little variation in response regardless of level then it was inconsequential as to the setting, but this fact allowed for flexibility if that setting was critical for one of the other response factors.

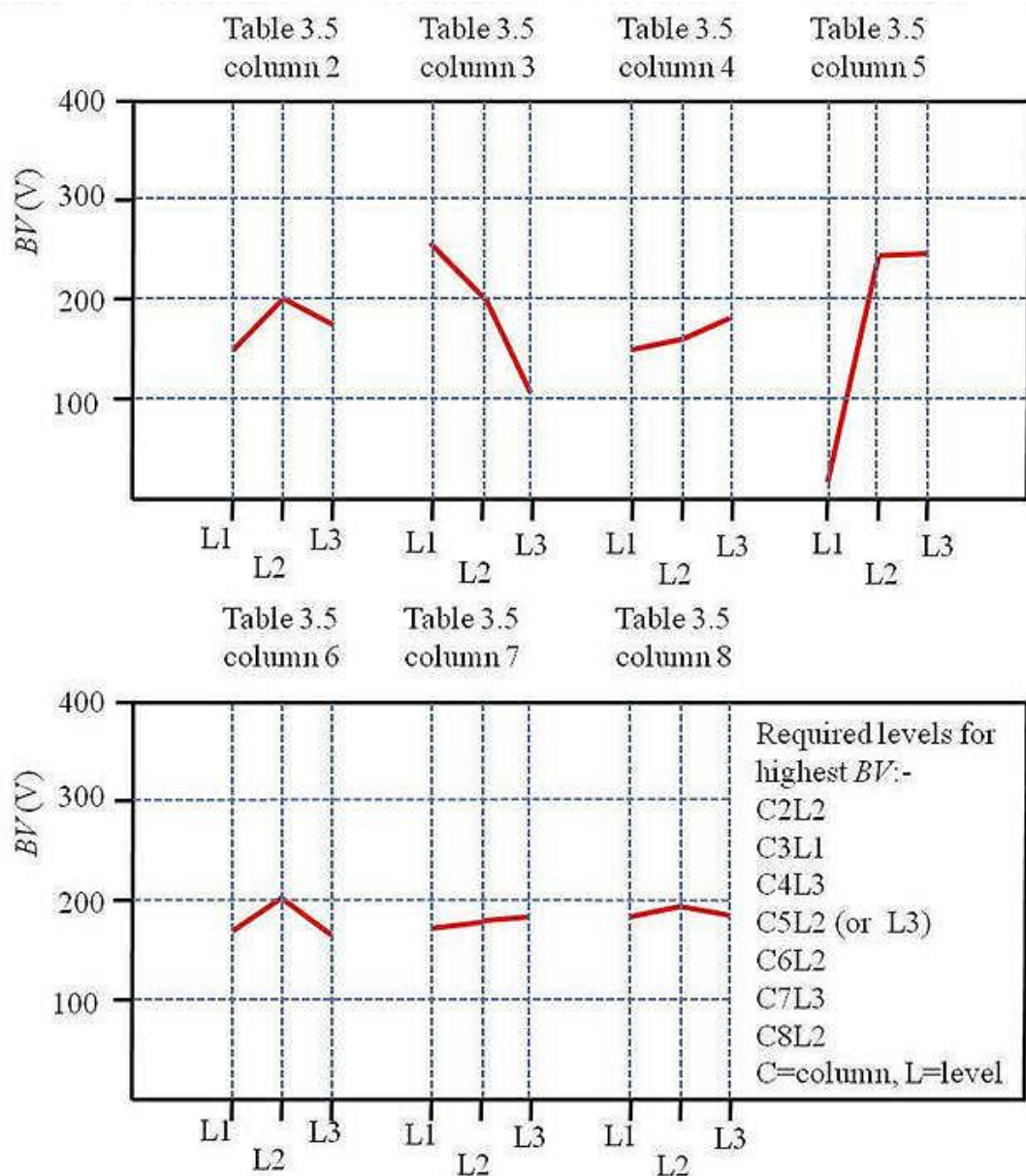


Figure 3.13. Mean response plots to obtain highest BV .

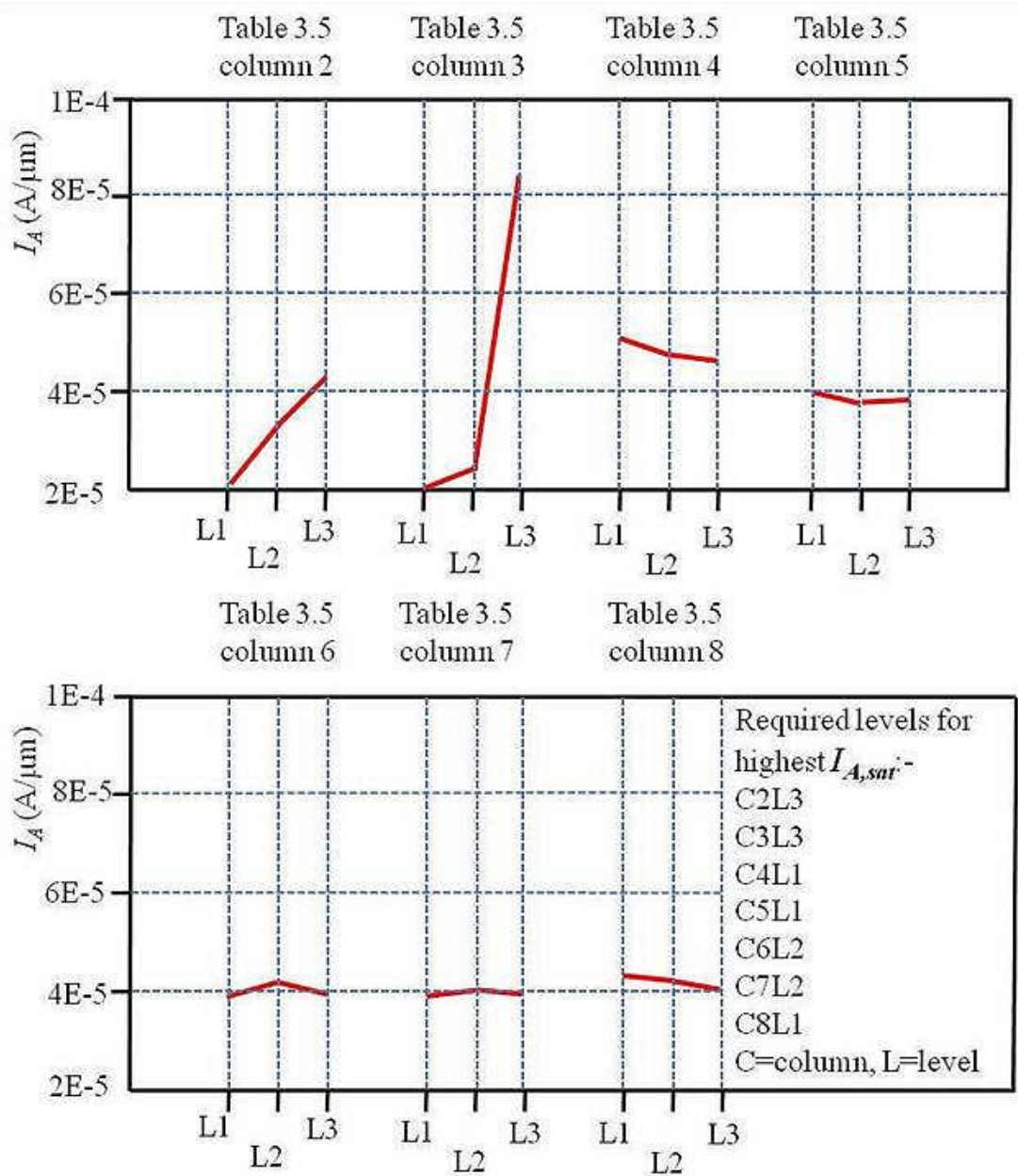


Figure 3.14. Mean response plots to obtain highest $I_{A,sat}$.

3.6.4 Best compromise and performance verification

The best compromise solution to the response factors is shown in table 3.8, particularly those affecting the higher priorities as shown in table 3.1. The performance of this best compromise solution could be predicted for any of the desired response factors such as BV or $I_{A,sat}$ using the Taguchi method as demonstrated in tables 3.9 and 3.10 respectively. The actual transfer characteristic data plot for MOSFET trial 19, the best compromise solution, is

shown in figure 3.15. As can be seen the predicted result and the actual result match for $I_{A,sat}$. The result for blocking voltage however, as shown in figure 3.16 was not matched, indeed there was a 35 % reduction from the predicted result. BV is notoriously difficult to predict however, as many factors influence the actual point at which avalanche occurs, for example the 2-dimensional affects of the P-body radius of curvature.

Control Factor	Column	Level	Value	Units
Cell width	2	3	5.5	μm
N-Drift doping	3	3	3.00E+15	cm^{-3}
P-body junction depth	4	1	1.25	μm
P-body surface concentration	5	2	3.00E+17	cm^{-3}
N+ cathode junction depth	6	2	0.2	μm
t_{OX}	7	2	2.00E-01	μm
Gate to cathode gap	8	2	0.1	μm

Table 3.8. Best compromise result for the VDMOSFET design as per the priorities shown in table 3.1.

Control Factor	Best compromise value	Units	Benefit
BV average			176
Cell width	174	V	(176-174) = 2
N-Drift doping	89	V	(176-89) = 87
P-body junction depth	156	V	(176-156) = 21
P-body surface concentration	253	V	(176-253) = -77
N+ cathode junction depth	203	V	(176-203) = -3
t_{OX}	181	V	(176-181) = -5
Gate to cathode gap	193	V	(176-193) = -17
Predicted outcome		V	(176-(-16))= 192

Table 3.9. BV prediction using best compromise VDMOSFET design.

Control Factor	Best compromise value	Units	Benefit
$I_{A,sat}$ average			4.21E-05
Cell width	5.77E-05	A/ μm	(4.21E-5-5.77E-5) = -1.56E-5
N-Drift doping	8.33E-05	A/ μm	(4.21E-5-8.33E-5) = -4.12E-5
P-body junction depth	5.24E-05	A/ μm	(4.21E-5-5.24E-5) = -1.03E-5
P-body surface concentration	4.01E-05	A/ μm	(4.21E-5-4.01E-5) = 2.00E-6
N+ cathode junction depth	4.89E-05	A/ μm	(4.21E-5-4.89E-5) = -6.8E-6
t_{OX}	4.34E-05	A/ μm	(4.21E-5-4.34E-5) = -1.3E-6
Gate to cathode gap	4.61E-05	A/ μm	(4.21E-5-4.61E-5) = -4E-6
Predicted outcome		A/ μm	(4.21E-(-7.73E-5)) = 1.19E-4

Table 3.10. $I_{A,sat}$ prediction using best compromise VDMOSFET design.

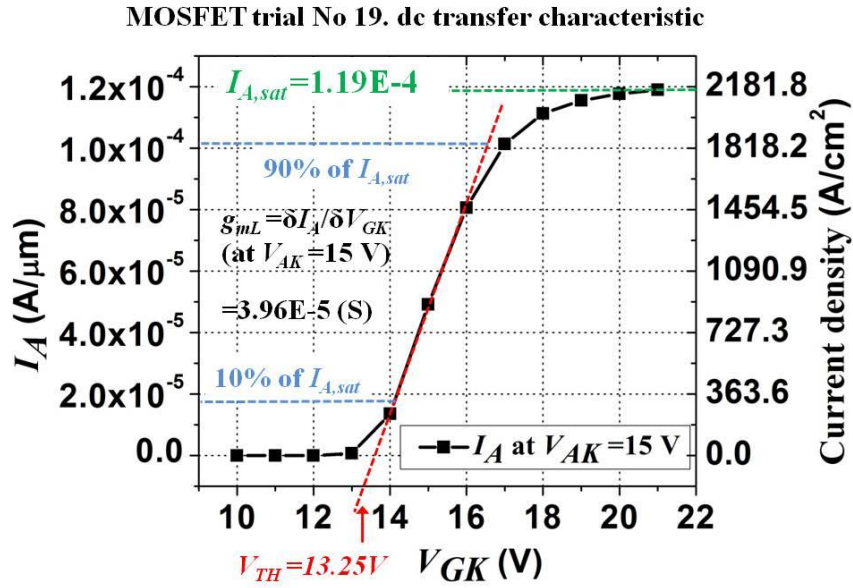


Figure 3.15. Best compromise resultant transfer characteristic.

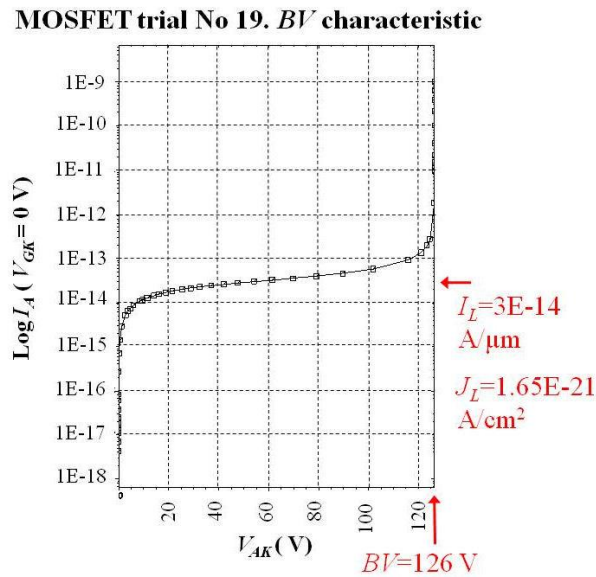


Figure 3.16. Best compromise resultant BV characteristic.

3.7 Enhancement of the best compromise design

The result of the DOE provided a best compromise result yielding a low on state static loss VDMOSFET with a BV within the target range of table 3.1 at 126 V with relatively low leakage of $J_L = 1.65E-21$ A/cm² at an isothermal lattice temperature of 300 K. The next stage

of development set out to reduce the V_{TH} . In addition the adjustment of the drift length from $D_L=25\mu\text{m}$, as used in the optimisation, to the minimum allowed by W_{DMAX} was necessary to further improve the conductivity of the best compromise result.

In order to reduce the threshold voltage a P-body type as described by Sze[10] called the retrograde implant structure was shown capable of reducing the surface N_a concentration and hence the threshold voltage (equation 3.10). The retrograde structure consisted of a low dose surface implant to obtain reduced V_{TH} whilst being protected by a higher dose deeper implant which provided the ability to reduce the depletion extent within the P-body to prevent punch through to the N+ cathode (equation 3.2 substituting N_a for N_d). Adjustment of the P-body however was likely to affect the BV , therefore the effect of adjusting the radius of curvature of the P-body required to be assessed.

3.7.1 Reduction in V_{TH} using a retrograde P-body

The required retrograde P-body design was similar to that created by Rung[24], wherein two acceptor ion implants were required: - one at a shallow depth of low dose (cm^{-2}) and one deeper using a higher dose as shown in figure 3.17. The benefits of a retrograde profile in a power MOSFET (albeit in a trench gate device) is described by Tsui[25]. The added benefits of the retrograde profile in addition to those identified in section 3.7 are that the voltage at which punch through occurred (V_{PT} , in terms of V_{AK}) is maintained (or increased) over the thermally diffused channel design of the same peak concentration (N_a), while the threshold voltage (V_{TH}) is reduced. The effective channel length (L_{eff}) as shown in figure 3.6 was also shortened, as V_{AK} was increased progressively (equation 3.2, substituting N_a for N_d), but in the retrograde channel L_{eff} was maintained at the point of highest N_a doping peak thus V_{PT} was increased. This occurred because the highest acceptor doping as shown in figure 3.17, occurred at approximately half way along the length of the channel in the X direction, unlike that of the thermally diffused profile where the highest concentration is at the cathode side of the channel. As regards to channel pinch off in the thermally diffused profile, as shown in figure 3.9, this would occur at the anode side of the channel where V_{TH} was lowest (due to

the coincidence with the lowest N_a concentration). According to Baliga[6] for the thermally diffused profile V_P (pinch-off voltage, in terms of V_{AK}) is shown in equation 3.22. In the case of the retrograde profile the channel length extended to the

$$V_P = V_{GK} - V_{TH} \text{ (V)} \quad (3.22)$$

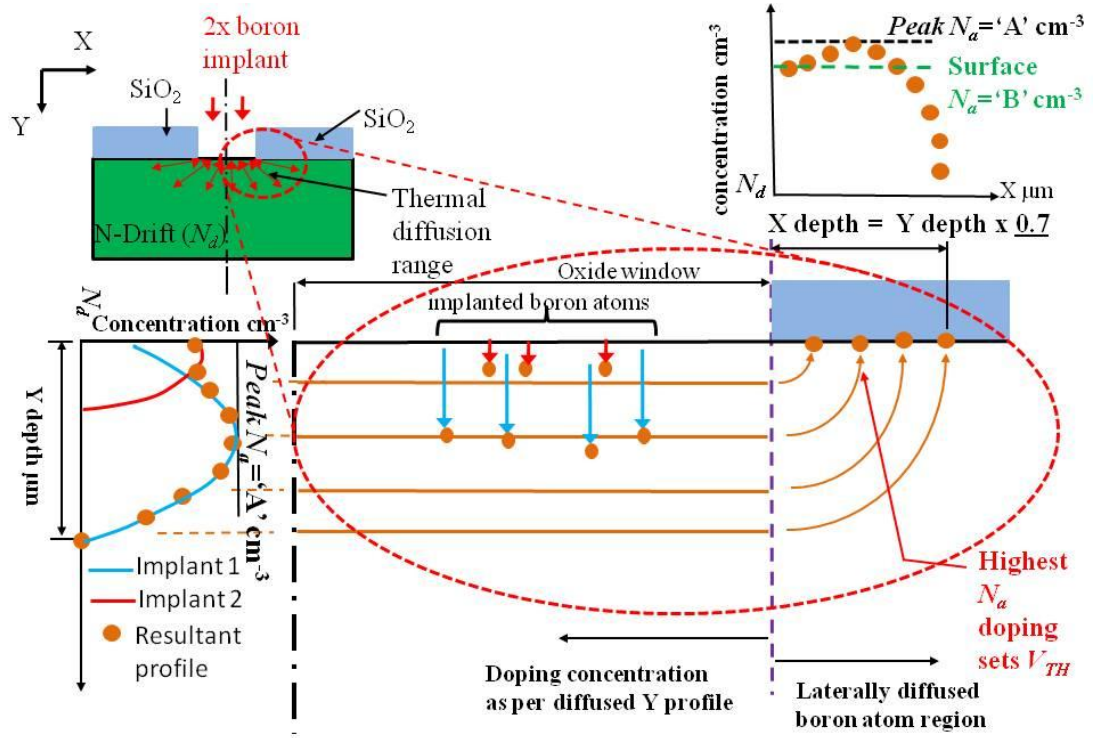


Figure 3.17. Ion implanted retrograde P-body profile in X and Y dimensions, Rotational factor =0.7, assumes no out diffusion in to SiO_2 .

point of highest acceptor doping at high V_{AK} . The lowest acceptor doping was at the N+ cathode side, the voltage developed along the length of the channel therefore was firstly reduced by the effective channel length and to cause pinch off was required to be higher than in the case of the thermally diffused profile due to the larger N_a doping at the anode side of the channel. Thus $I_{A,sat}$ was increased using the retrograde profile when compared to the thermally diffused profile.

The resultant doping profiles in both X and Y dimensions are shown in figure 3.18 as a direct comparison between the surface doped thermally diffused P-body profile and the ion implanted and short duration annealed retrograde P-body. Please note that in this instance the channel length L_{CH} was artificially adjusted from that of a self aligned structure in order to ensure that L_{CH} was the same (0.5 μm) in both the thermally diffused and retrograde P-bodies by shifting the N+ cathode of the model with the retrograde profile.

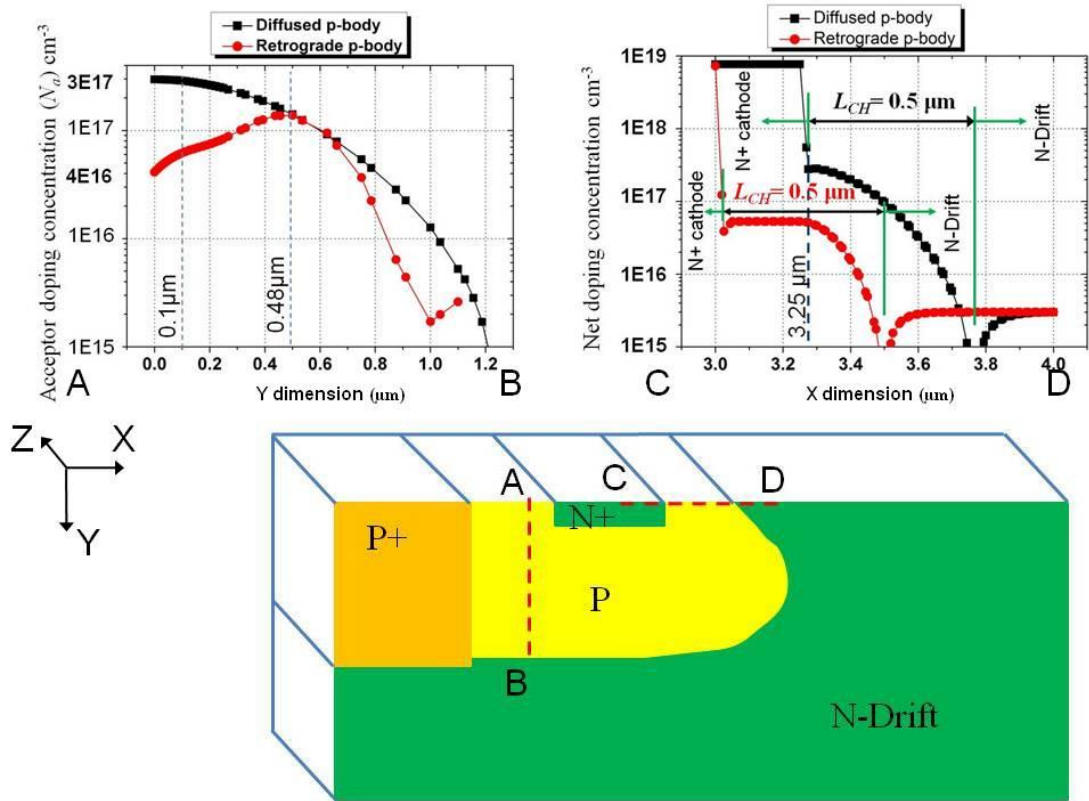


Figure 3.18. Comparison of surface doped (thermally diffused) and ion implanted retrograde P-body profiles in X and Y dimensions, assuming no out diffusion.

Otherwise the reduced L_{CH} of the retrograde profile would result in punch through as the channel length was too small for the blocking voltage rating of $BV \approx 120$ V. The comparison of the resultant transfer characteristics can be seen in figures 3.19 and 3.20.

As can be seen from figure 3.19 the retrograde profile reduced the V_{TH} of the original surface doped and thermally diffused profile from $V_{TH} = 13.25$ V to $V_{TH} = 5$ V. If using the same measure as used in the optimisation then a shift of -8 V was due entirely to

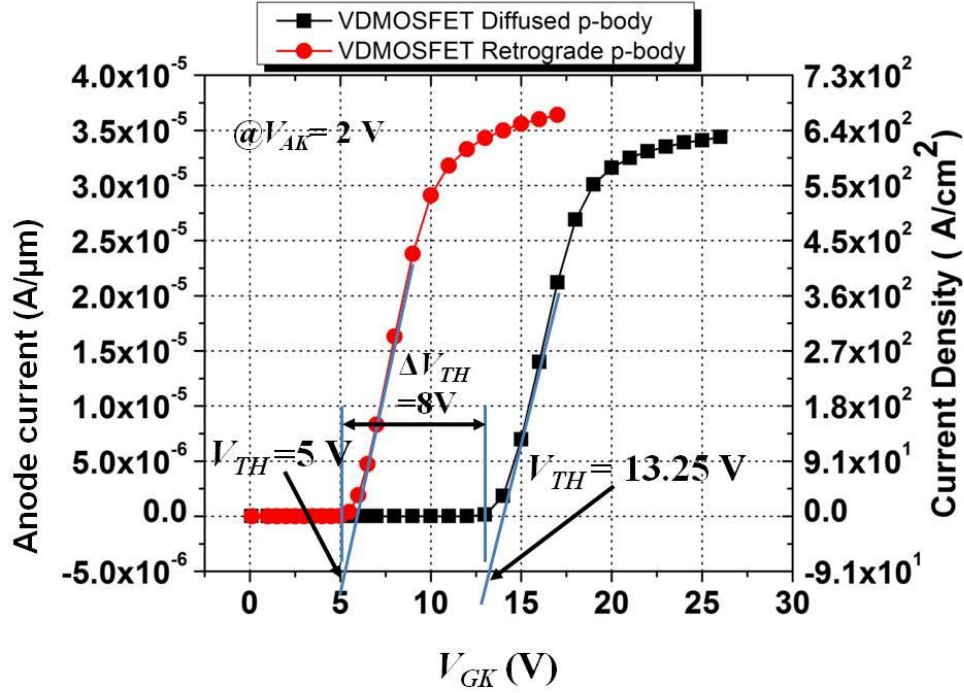


Figure 3.19. Comparison of transfer characteristic at $V_{AK}=2$ V for the compared P-body profiles of figure 3.17 (Linear Y axis).

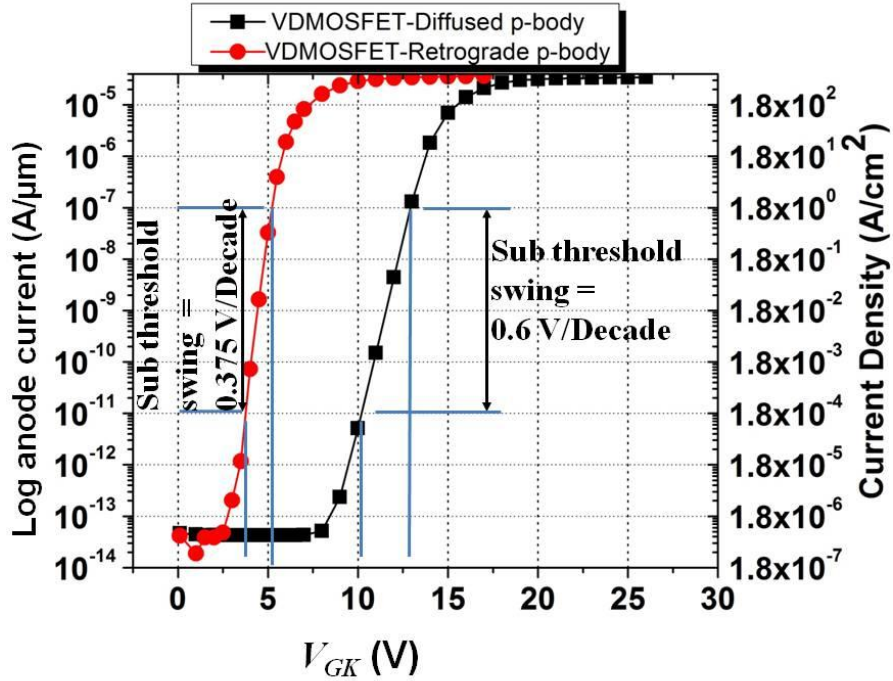


Figure 3.20. Comparison of transfer characteristic at $V_{AK}=2$ V for the compared P-body profiles of figure 3.17 (Log₁₀ Y axis).

the reduced N_a of the channel as shown in figure 3.18. The comparison of the calculated V_{TH} for both the diffused and retrograde profiles is shown at Appendix 2.1 and 2.2 respectively, the calculated values predicted a larger downward shift of 11.39 V, but this did not take into

account any factors influencing the flat band voltage (V_{FB}). In addition $I_{A,sat}$ of the retrograde structure was improved over the thermally diffused structure due to L_{eff} and the V_{TH} reduction (as predicted from equation 3.12). Similarly, as predicted the sub threshold swing, as shown in figure 3.20, was improved in the retrograde structure by almost a factor of 2 over that of the surface doped thermally diffused profile in that it was much more abrupt in terms of V_{GK} .

3.7.2 Blocking voltage assessment

The effect of the revised P-body on the BV required to be assessed due firstly to the amended P-body 1-D doping profile as shown in figure 3.18, but secondly due to the 2-D effects brought about by the change to the radius of curvature (r) as shown in figure 3.21. In addition a self aligned variant of the retrograde P-body structure was also analysed, although in this case the contacts of structure c) were simply repositioned relative to the same doping profiles declared in structure b).

The resulting BV for each of the compared structures of figure 3.21 can be seen in figure 3.22, otherwise all the structures were identical. The 1-D results were obtained using the P-body doping shown in figure 3.18, (cut A to B) with N-Drift doping, $N_d = 3E15 \text{ cm}^{-3}$. As can be seen the main difference was that of leakage current between the 1-D and 2D results, leakage being slightly larger for the 2-D results due to the increased electric field at the radius of curvature. The other difference was that in all cases the 2-D result provided an increased point of avalanche in terms of V_{AK} over that of the 1-D result. This was due to the increased volume of N-Drift region directly under the gate electrode in the 2-D structure which meant that the charge was more distributed hence for the same ϵ_{MAX} the area under the electric field plot provided a slightly increased voltage prior to avalanche relative to the 1-D result. From these results it was concluded that the retrograde P-body was not detrimental to the BV rating of the optimised VDMOSFET, the slightly reduced BV was more than offset by the improvements to $I_{A,sat}$, V_{TH} , and sub threshold swing.

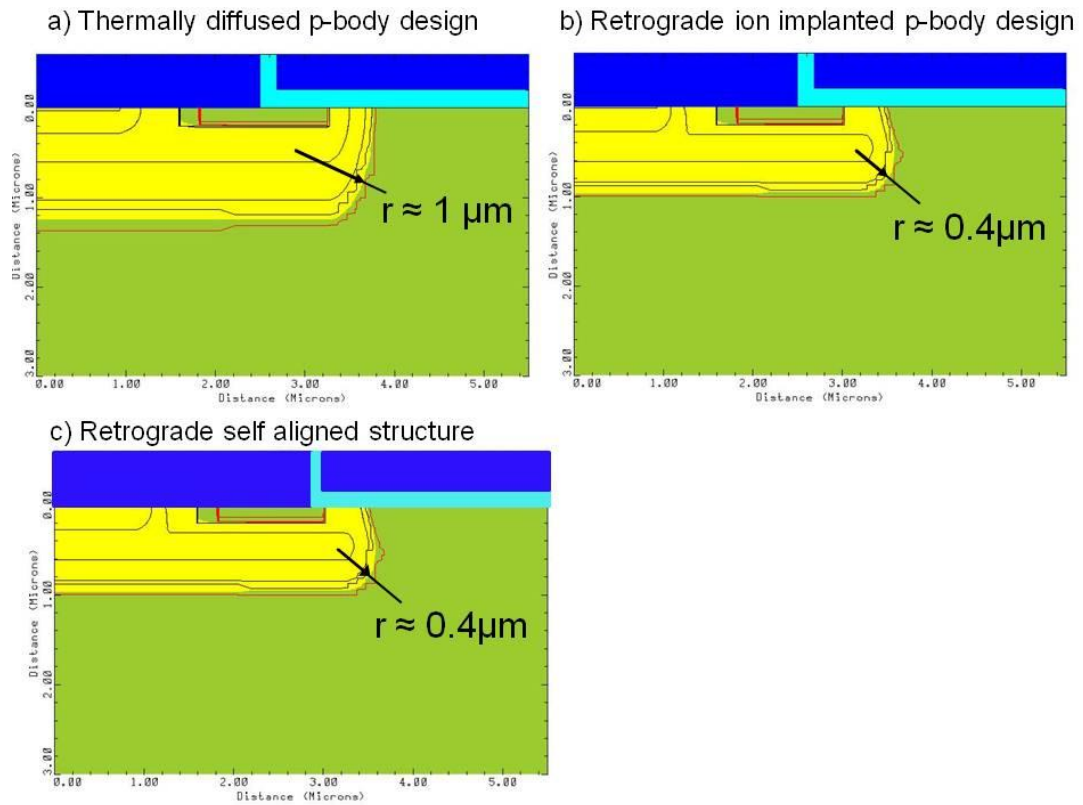


Figure 3.21. Variation in radius of curvature between the thermally diffused and retrograde P-body profiles.

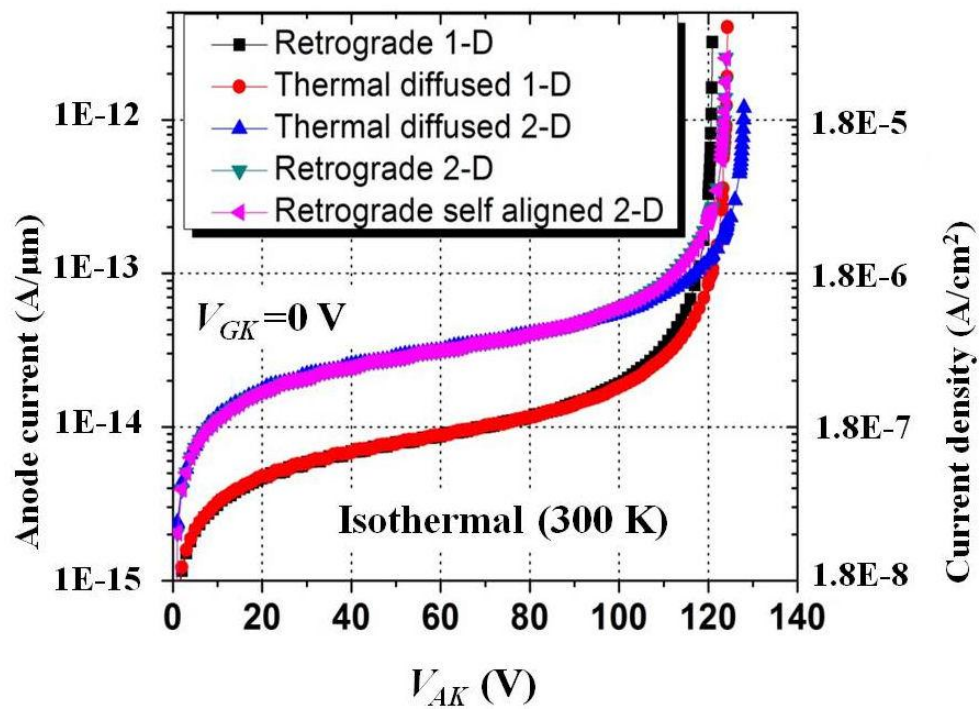


Figure 3.22. Effect of the various P-body designs of figure 3.21 on BV.

3.7.3 Drift length reduction

Having optimised the VDMOSFET in terms of cell dimensions, doping and channel length the effect of the drift length reduction from 25 μm to 12 μm can be seen in figure 3.23.

Clearly the resistance given by the slope of the I-V characteristic linear region is much reduced with $D_L=12\ \mu\text{m}$. As shown in figure 3.24 there was also further scope for drift

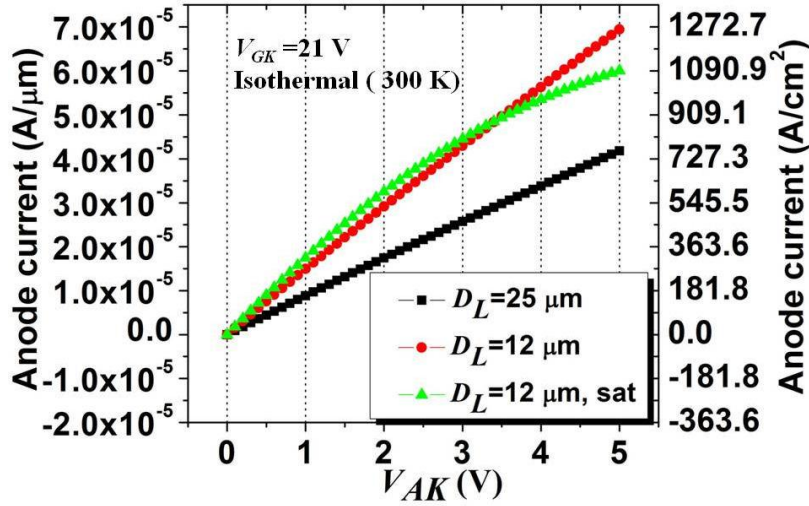


Figure 3.23. Effect of drift length (D_L) reduction on VDMOSFET forward I-V characteristic.

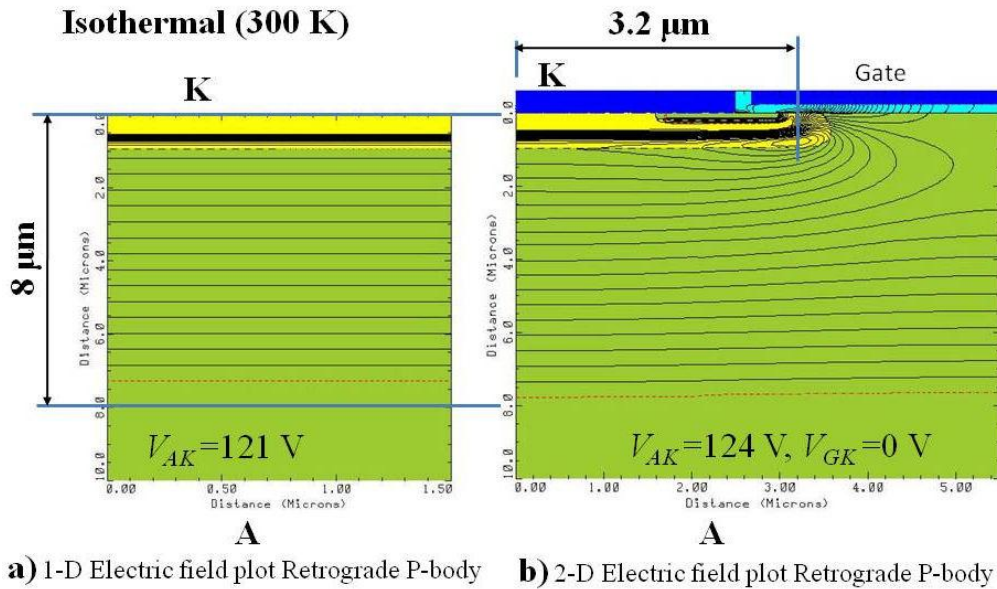


Figure 3.24. Electric field contour plot of the optimised a) 1-D and b) 2-D VDMOSFET structures with ($V_{GK}=0\ \text{V}$) showing $W_{D\text{MAX}}=8\ \mu\text{m}$ at $\epsilon_{\text{MAX}}=\epsilon_{\text{CRIT}}$.

length reduction as at ε_{MAX} , $W_{D_{MAX}} \approx 8 \mu\text{m}$ if required. An additional plot is provided in figure 3.23 called “ $D_L=12 \mu\text{m}$, sat”, this result was from the identical optimised structure, but on this occasion the reduction in structure dimensions allowed additional refinement of the grid in the channel area to enable the channel saturation to be plotted accurately for the first time.

3.8 Body diode performance

The body diode performance of a MOSFET is often critical to switched applications incorporating inductive loads as the required separate diode used to conduct the MOSFET switched inductive current, post turn off, can often be omitted if the P-body diode within a MOSFET is good enough in terms of conduction losses, recovery time (in the event of avalanche) and turn on time. The switching characteristics have not been evaluated within this chapter, but the body diode forward voltage for a given anode current is to be minimised. According to Barkhordarian[26] the typical forward voltage of the body diode within a MOSFET is around 1 V for a BV of around 100 V, increasing to 1.6 V for $BV > 100$ V. This is similar to the VDMOSFET of this work as shown in figure 3.25, although this forward voltage is also temperature dependant due to the temperature effects on the Fermi levels as shown in figure 3.26 (as described by Sze[10]), which in turn affects the built in voltage (V_{BI}) of the P-N junction.

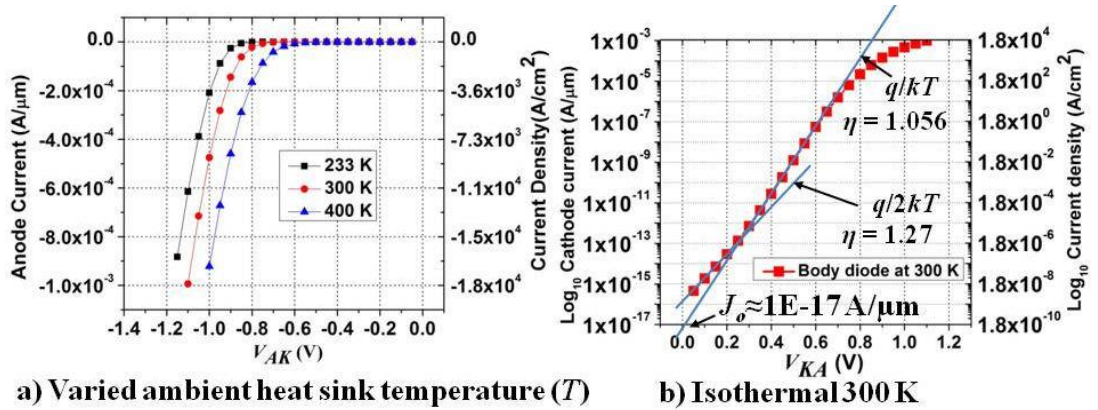


Figure 3.25. Review of body diode performance for the self aligned retrograde P-body VDMOSFET model.

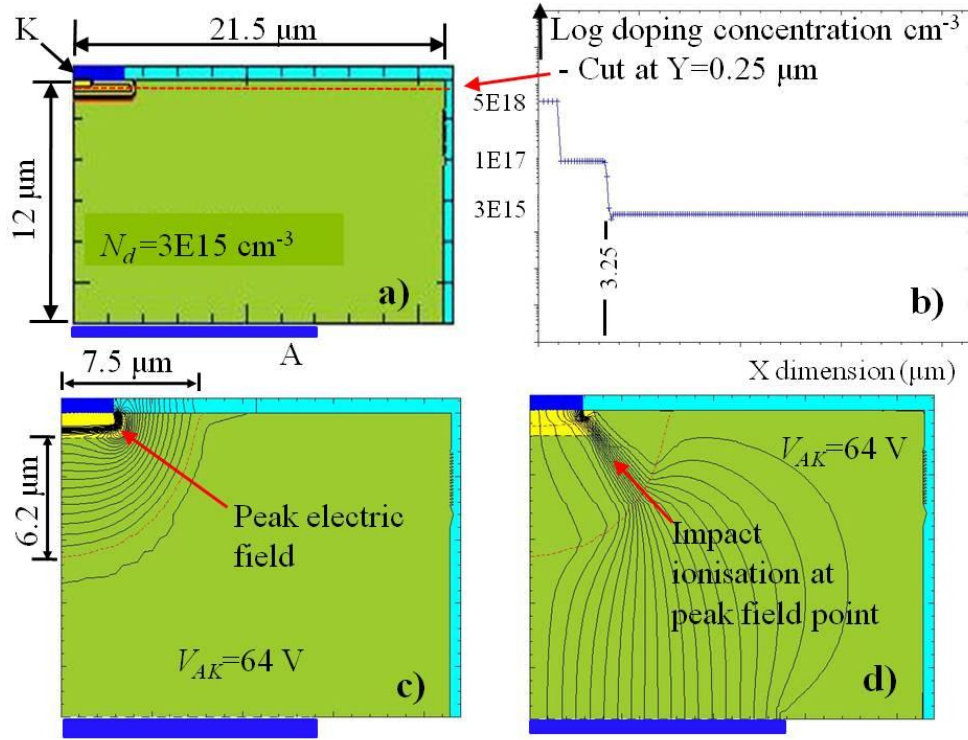


Figure 3.27. Radius of curvature effect at device edge: a) Structure to assess avalanche, b) log plot of doping concentration, c) electric field plot at avalanche, d) 5 % current flow lines at avalanche.

too far from the planar junction very little of the potential is transferred to it, and the breakdown occurs due to field crowding at the planar junction. If the field ring is placed too close to the planar junction most of the potential is transferred to it, and breakdown occurs due to field crowding at the field ring. With optimal field ring spacing breakdown occurs simultaneously at the planar junction and the field ring.

The potential developed laterally across a single floating ring (V_{FFR}), in the case where the P-body depletion extent has met the floating ring is shown at equation 3.23. This comes from the Poisson equation as shown in equation 3.2 and the voltage solution shown at equation 3.5, in figure 3.2.

$$V_{FFR} = \frac{qNd}{K_s \epsilon_o} \left(W_{DMAX} W_s - \frac{W_s^2}{2} \right) \quad (3.23)$$

The field ring spacing was given the suffix W_s by Baliga[6], who stated that for a $BV \leq 50$ V then one ring was sufficient however, at higher BV then multiple rings were required. Essentially, the electric field developed at the edge of the first floating ring can be reduced if surrounded by another floating ring. A smaller distance W_s was favoured with a multiple ring design relative to a single ring optimum according to Baliga[6].

For the multiple ring design used in this work W_s was a variable which formed the identical gap between each separate implant window, and the oxide window width of each ring was fixed at $1 \mu\text{m}$, again a rotation factor of 0.7 was used. A similar structure was also described by Baliga[6] which used less silicon area utilised varied spacing (W_s) and varied floating ring width.

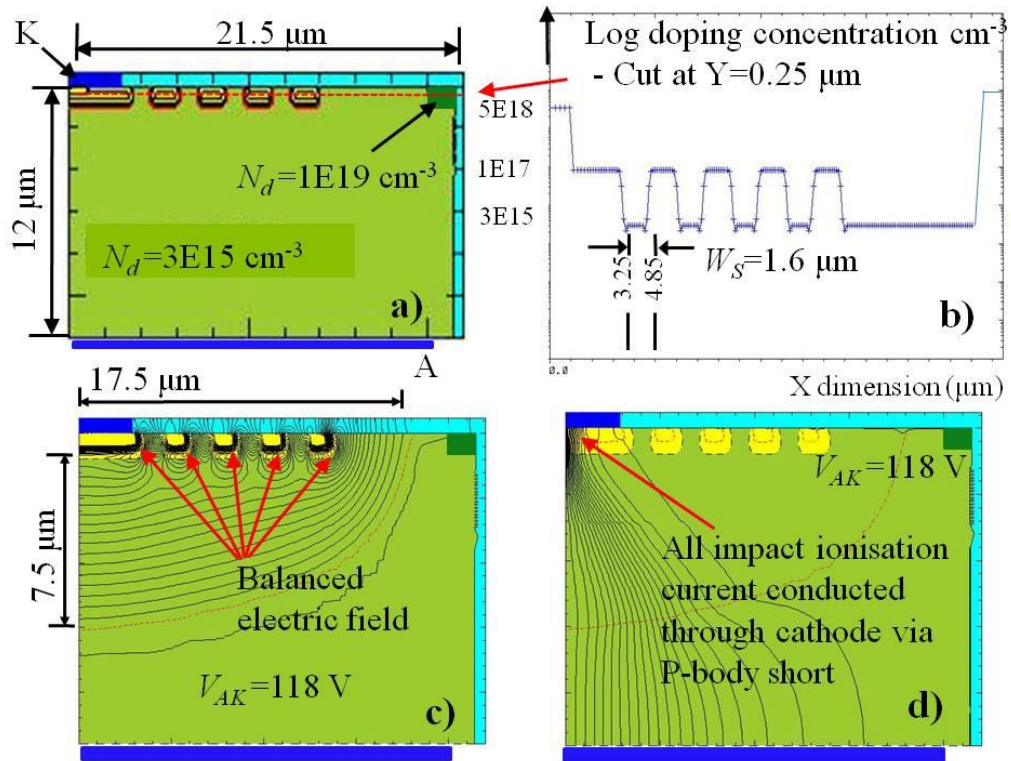


Figure 3.28 Optimum value of W_s : a) Structure to assess avalanche, b) log plot of doping concentration, c) electric field plot at avalanche, d) 5 % current flow lines at avalanche.

An iterative approach to the multiple floating field ring design started with $W_s = 2.25 \mu\text{m}$ the optimum was then sought in the range $1.5 > W_s < 2.25 \mu\text{m}$. The aim was to locate the

distance at which breakdown occurred simultaneously in all the rings and the bulk. The optimum dimension was found to be where $W_S = 1.6 \mu\text{m}$ as shown in figure 3.28. This was proven as the resultant electric field peaks in terms of magnitude (V/cm) was balanced across all the floating rings and the radius of curvature as shown in figure 3.28 c). As a balance existed, in terms of the electric field peaks in each ring and the P-body, then the entire impact ionisation hole current flowed via the lowest resistive path to ground (the P-body to cathode short) as shown in figure 3.28 d). The blocking voltage achieved was 118 V this can be seen in comparison to the theoretical or 1-D doping dependant result in figure 3.29.

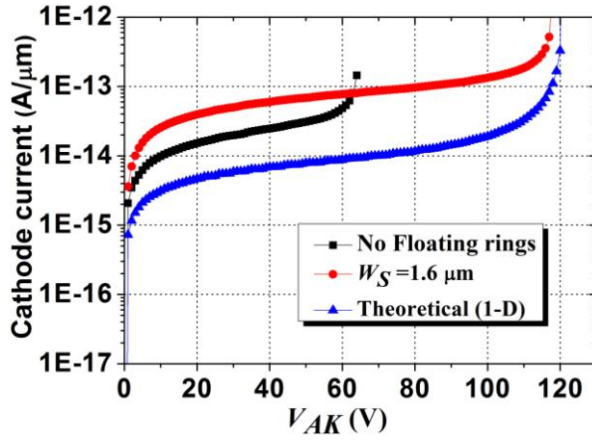


Figure 3.29. Direct comparison of I-V characteristics for the optimised floating ring design with the unprotected radius of curvature and the theoretical doping dependant characteristic.

3.10 Compared measures of performance

The resultant forward characteristics of the finalised VDMOSFET, with the self aligned retrograde P-body, are shown in figure 3.30 using a selection of gate bias (V_{GK}).

A current reading taken at $V_{AK} = 2 \text{ V}$ (approximately in the middle of the linear region) was used to calculate the specific on state resistance for the finalised VDMOSFET model. The calculation is as follows:-

$$R_{(ON)} = \frac{V_{AK}}{I_A} = \frac{2}{3.55E-5} = 56.33 \text{ k}\Omega \quad (3.24)$$

$$R_{(ON,SP)} = R_{(ON)} * A = 56.03E3 * 0.055E-6 = 3.098 \text{ m}\Omega\text{cm}^2 \quad (3.25)$$

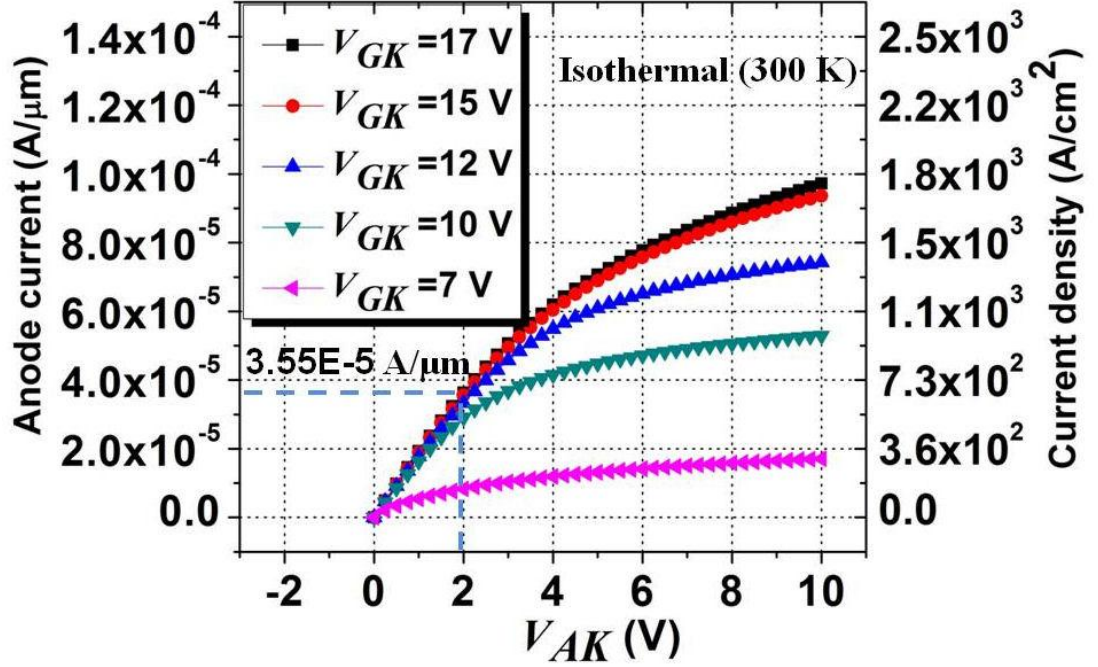


Figure 3.30. Forward characteristic of the finalised VDMOSFET.

To provide a comparison in terms of $R_{(ON,SP)}$ with commercially available devices proved difficult as the active area of the commercial chip is normally undisclosed in manufacturers data. Instead a search for papers was completed which contained a directly comparable VDMOSFET modelled structure with a BV in the region of 120 V, resulting in a paper by Shuming[30]. This paper contained all the necessary information to calculate $R_{(ON,SP)}$ of a VDMOSFET at a BV of 82 V. Unfortunately, from the dc characteristics plot provided by Shuming[30] the result calculated to units of $\mu\Omega\text{cm}^2$ with $V_{AK}=2$ V, which for an N-Drift doping of $N_d=2.5E15 \text{ cm}^{-3}$, with a thickness of 9 μm , was impossible. Calculations instead were made to obtain the N-Drift resistivity and from those calculate the theoretical minimum $R_{(ON,SP)}$ for the given cell area (which did not include the channel, accumulation and JFET resistance). Calculations were as follows:-

$$\rho = \frac{1}{q\mu_n N_d} = \frac{1}{1.6E-19 * 1200 * 2.5E15} = 2.08 \Omega\text{cm} \quad (3.26)$$

$$R_{(ON)} = \rho \frac{L}{A} = 2.08 \left(\frac{9E-4}{8.25E-8} \right) = 22.69 \text{ k}\Omega \quad (3.20)$$

$$R_{(ON,SP)} = R_{(ON)} * A = 1.872E-3 \Omega\text{cm}^2 \quad (3.27)$$

Where A= 1E-4 cm*8.25E-4 cm, $N_d = 2.5E15 \text{ cm}^{-3}$, $\mu_n \approx 1200 \text{ cm}^2/\text{V-s}$, L=9E-4 cm

The above result may however, be subject to incorrect assumptions, such as the assumption concerning the cell thickness in the Z dimension. For the purposes of comparison a point was recorded on to $R_{(ON,SP)}$ versus BV plot as shown in figure 3.31. In addition a number of points were also added to figure 3.31 in order to provide a comparison of other MOSFET, or potential other MOSFET replacement device technologies. The potential benefit to the silicon design of using super junction or charge balance technology is demonstrated by the device reported by Saito[31]. In addition the use of the wide band gap materials such as silicon carbide, allowed for a 1200 V MOSFET design with low on state loss within a power module as reported by Stevanovic[32]. Unfortunately, as explained in chapter 2, such wide band gap devices presently do not meet the required cost performance benefits for widespread commercial usage due to the costly vapour phase crystal growth. Currently no work has yet demonstrated a Vertical MOSFET performance in SiC which matched the theoretical performance of the material due to mobility issues within the channel as discussed by Matocha[33]. One final comparison device was also added which was fabricated from another possible wide band gap material to provide a high blocking voltage called gallium nitride (GaN) as reported by Saito[34]. Unfortunately, GaN is also far from an ideal material as discussed by Chow[35], particularly as GaN High Electron Mobility Transistors (HEMTs) are normally on devices and bulk GaN substrates are more expensive than SiC, thus restricting the use of GaN to producing lateral devices only, using layers of GaN which are grown on sapphire, silicon carbide and now low cost silicon substrates.

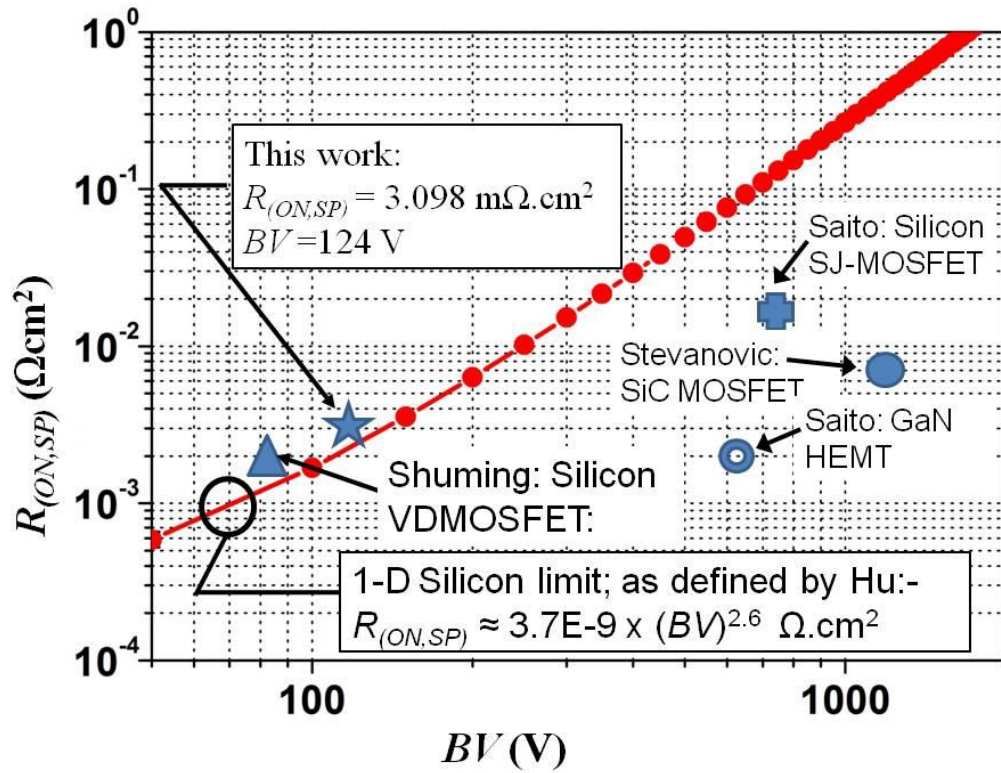


Figure 3.31. Comparison of specific on state resistance versus Blocking Voltage for the finalised silicon VDMOSFET design.

3.11 Chapter Summary

Within this chapter a VDMOSFET model was developed and optimised for lowest on state resistance while maintaining a minimum level of Blocking Voltage. The achieved measures of performance achieved were a specific on state resistance of $3.098 \text{ m}\Omega\text{cm}^2$ with a Blocking Voltage of 124 V. The resultant model could therefore form the basis of the subsequent development of the injected bipolar (or hybrid device) in which the design goal was to provide reduced on state loss in the event of surge or fault current levels.

3.12 References

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Chapter 4 | Achieving bipolar conduction

4.0 Introduction

Having achieved an optimised low loss unipolar VDMOSFET design in the previous chapter, the benefits of achieving self biased bipolar conduction within a MOS gated structure of similar Blocking Voltage rating will be described within this chapter. Firstly, a brief description will be provided about what it means to achieve a high injection state within a semiconductor. Four methods of injecting minority carriers will then be described as related to commercially available and state of the art device types.

Following the introductory review of what the injected state means and how minority carrier injection may be provisioned within a VDMOSFET structure to achieve conductivity modulation then the added benefit of achieving bipolar conduction will be described. One minority carrier injection method will be chosen to demonstrate both conductivity modulation and bipolar conduction and a review of the role of the ideal structure to achieve that will be completed.

The ultimate intension for the use of such a self biased injector is to enable an ‘on demand’ reduced resistance state to augment the VDMOSFET performance in case of excessive current demand from a load which has either gone short circuit, or during turn on requires the charging of capacitors, known as ‘surge current’. With the use of figure 3.30 of Chapter 3 then the effect of a conductivity modulated state within a VDMOSFET structure will be to break the silicon limit line and therefore obtain a lower specific on state resistance ($R_{ON,SP}$) for a given blocking voltage (BV).

4.1 The high injection state

The following section briefly describes what it means to achieve a high injection state within a semiconductor power switching device, that is, to excite a semiconductor into being an improved conductor. The equilibrium state within a semiconductor was described by Grove[1], known as the mass-action law as follows:-

$$pn = n_i^2 = N_C N_V e^{-\frac{E_G}{kT}} \quad (4.1)$$

Where for Silicon: n_i = intrinsic carrier concentration ($9.65 \times 10^9 \text{ cm}^{-3}$), N_C = effective density of states in the Conduction band ($2.8 \times 10^{19} \text{ cm}^{-3}$), N_V = effective density of states in the Valance band ($2.65 \times 10^{19} \text{ cm}^{-3}$), E_G = Energy gap (1.12 eV), k = Boltzmann constant ($8.6174 \times 10^{-5} \text{ eV/K}$), T = temperature (K), after Sze[2].

Obviously, the absolute quantities of the carriers are temperature dependant, but also N_C and N_V themselves are temperature dependant, according to Grove[1].

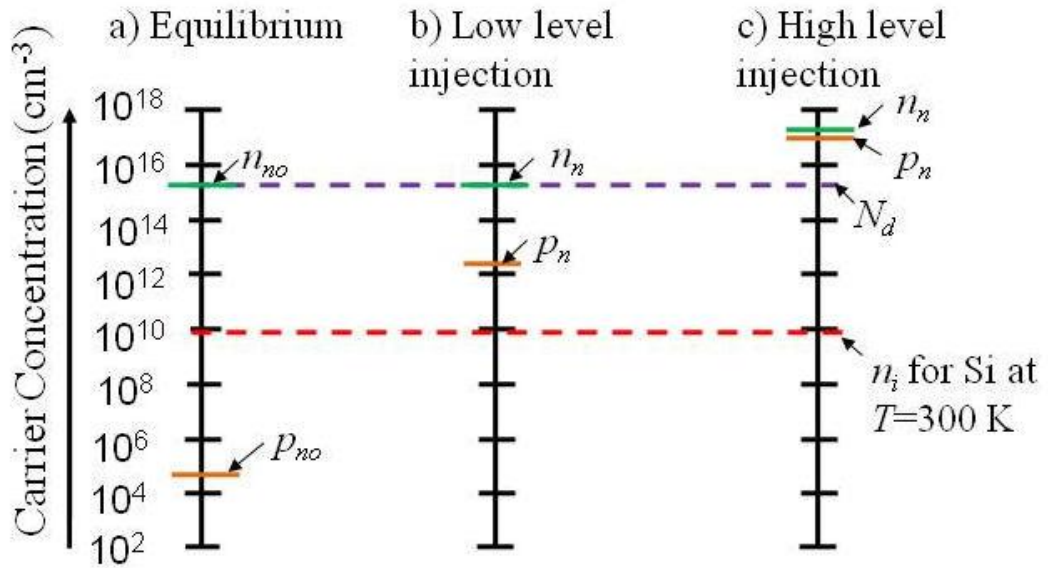


Figure 4.1. The relative concentrations of holes and electrons in an n-type semiconductor (doped to $3 \times 10^{15} \text{ cm}^{-3}$) under three conditions; a) equilibrium, b) low-level injection and c) high level injection. After Grove[1].

Injection was described by Grove[1] to be the increase in carriers from the equilibrium state (where n_{no} is the electron and p_{no} is the hole concentration at equilibrium, as shown within figure 4.1). Such an increase from n_{no} and p_{no} essentially violates the mass action law, hence $np \neq n_i^2$, the initial level of which is described by low level injection where the increase from p_{no} to p_n is insufficient to cause any change in the electron concentration

(hence $n_n = n_{no}$). Upon excitation in to a high level injected state then an extremely large increase in minority carriers (p_n) can cause an increase in majority carriers (n_n) over and above the donor concentration thus, high level injection is often referred to as conductivity modulation, in that the semiconductor has been excited in to a higher conductivity, or lower resistance, state. As a ‘rule of thumb’, high level injection is said to exist when $p_n > n_{no}$ by approximately 10 %. Although the increase is temporary the effect is similar to having doped the semiconductor with increased donors in the case of n-type material. Therefore if conductivity modulation of the VDMOSFET structure is obtained, which in effect increases the donor concentration from $3E15 \text{ cm}^{-3}$ to $1E17 \text{ cm}^{-3}$, the expected reduction in resistance, $R_{(ON)}$, for the N-Drift region within a unipolar VDMOSFET is calculated as follows:-

$$\rho = \frac{1}{q\mu N_d} = \frac{1}{1.6E-19 * 1225 * 3E15} = 1.7 \quad \Omega.\text{cm} \quad (4.2)$$

$$\rho = \frac{1}{q\mu N_d} = \frac{1}{1.6E-19 * 750 * 1E17} = 0.083 \quad \Omega.\text{cm} \quad (4.3)$$

For a cell area $10 \mu\text{m} \times 1 \mu\text{m}$ and epitaxial layer thickness of $10 \mu\text{m}$ the resistance can be calculated as follows:-

$$R_{(ON)} = \rho \frac{L}{A} = 1.7 \cdot \frac{10 * 1E-4}{10 * 1E-4 * 1E-4} = 17 \quad \text{k}\Omega, \quad (4.4)$$

$$R_{(ON)} = \rho \frac{L}{A} = 0.083 \cdot \frac{10 * 1E-4}{10 * 1E-4 * 1E-4} = 830 \quad \Omega, \quad (4.5)$$

Hence, a considerable reduction in on state resistance within a VDMOSFET drift region is available if the state of conductivity modulation can be achieved. To achieve a state of conductivity modulation a minority carrier injector of some form is required. Ideally this minority carrier injector should be externally connected to a positive voltage supply, and yet be entirely self-biased in terms of developing the necessary internal charge profile to enable forward bias of the P-Anode injector to N-Drift junction to enable minority carrier injection to occur in response only to external bias in terms of anode to cathode voltage (V_{AK}) applied to the terminals.

4.2 Minority carrier injection methods

The injection of minority carriers can be achieved via one of four methods into an N type silicon region such as the N-Drift region (with $N_d=3E15 \text{ cm}^{-3}$) of the optimised VDMOSFET resulting from chapter 3:-

- 1) The forward biasing of a P-N junction.
- 2) The forward biasing of a Schottky junction.
- 3) The forward biasing of a Junction Barrier Schottky diode (JBS) diode (a hybrid of 1, and 2 above).
- 4) The accumulation layer of an enhancement P-MOS channel can also be used.

Each of these 4 methods will be described separately within this section.

4.2.1 Minority injection from a P-N junction

A description is available from many sources, such as Parker[3], Pierret[4] Grove[1], and Sze[2], of the forward biasing of a P-N junction diode which will allow a large diffusion current to flow as a result of the reduction of a potential barrier via forward biasing the P-N junction. Once the barrier is reduced then holes from a highly doped region are allowed to diffuse into the relatively low doped donor region.

As the implanted retrograde profile was to be used for the P-body of the MOSFET as described in Chapter 3, it is convenient to use the same implant to form an injector, thus reducing the number of masks needed. In addition this P-Anode design was compared to an implant with increased acceptor doping concentration, as shown in figure 4.2. Both profiles were described and created as a structure suitable for simulation using the Synopsys Medici simulator[5].

The resultant linear scaled current–voltage (I-V) characteristic of the highly doped profile ($1E20 \text{ cm}^{-3}$) in comparison to the implant discussed earlier which peaked at $1.15E17 \text{ cm}^{-3}$ is shown in figure 4.3, the response plotted against a log Y scale is shown in figure 4.4.

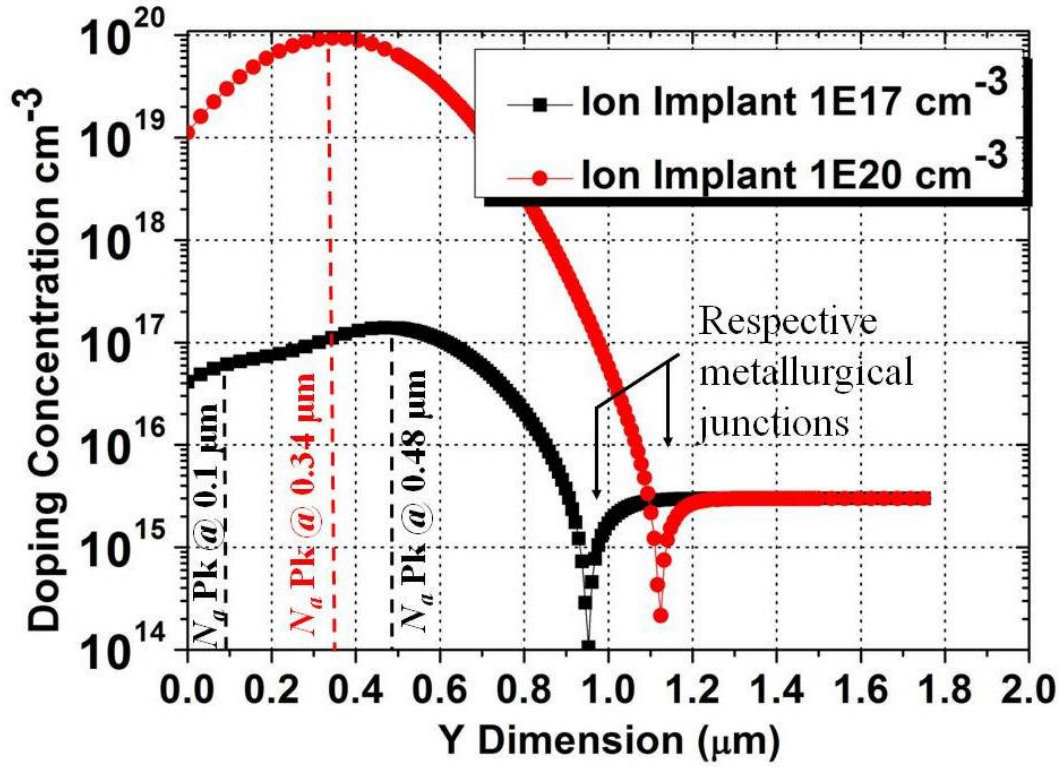


Figure 4.2. Comparison of ion implanted profiles for the acceptor doped region.

If the bias at which forward conduction occurs on the linear scale is termed V_i (when $V_{AK}=V_i =V_{BI}$) then the increase in V_i is readily apparent as a result of the increase in doping level as shown in figure 4.3. As can be seen from the I-V characteristic plotted against a log scale (figure 4.4) the higher peak doping now provides a change in slope of the I-V characteristic due to the change from q/kT to $q/2kT$. This is an indication that a high injection level has been achieved with the $N_a=1 \times 10^{20} \text{ cm}^{-3}$ peak doping. In the high injection state the ideal diode equation becomes that shown in equation 4.6, according to Sze[2].

$$J = J_p + J_n = J_o \left[\exp \frac{qV_{AK}}{2kT} - 1 \right] \quad (\text{A}) \quad (4.6)$$

Where J is the total current density, J_n is the electron current density, J_p is the hole current density, J_o is the saturation current density.

The estimated V_{BI} obtained for the higher and lower doped implants from figure 4.3) are of the same order as those calculated, as shown at Appendix 3.1 (equations A3.1.2 and A3.1.3 respectively) so these had simulated correctly. Similarly, the calculation of the saturation current (I_o) for the model with the peak doping of $N_a=1.15 \text{E}17 \text{ cm}^{-3}$ is shown at Appendix

A3.2. The calculated result was $I_0=2.568\text{E-}18\text{ A}/\mu\text{m}$ (using equation A3.2.8) whereas the result plotted in figure 4.4 gave a result in the region of $I_0=8\text{E-}18\text{ A}/\mu\text{m}$. The theoretical calculation however, assumed a uniform profile set at $1.15\text{E}17\text{ cm}^{-3}$ so this result was acceptable and the simulation was deemed good.

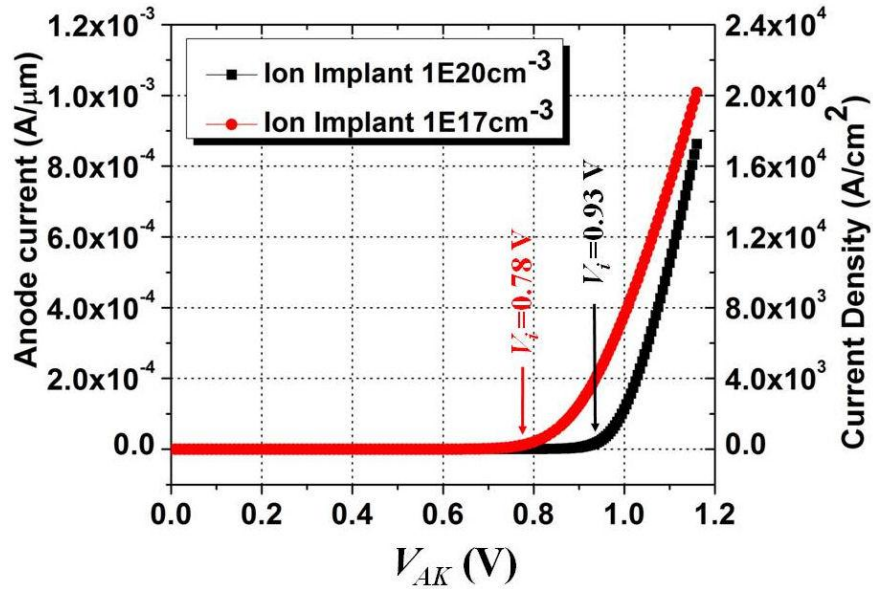


Figure 4.3. Comparison of I-V characteristics between two ion implants of different peak concentration plotted against a linear Y scale. Isothermal ($T=300\text{ K}$).

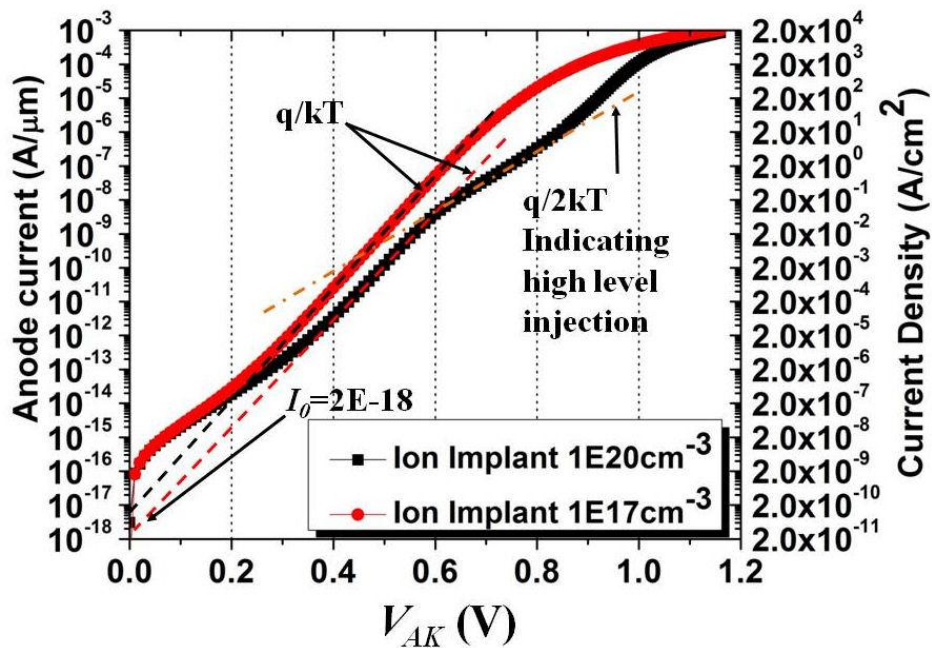


Figure 4.4. Comparison of I-V characteristics between two ion implants of different peak concentration plotted against a log Y scale.

A comparison of the hole and electron concentrations throughout the P-N junction diode is shown in figures 4.5 and 4.6, wherein figures 4.5 a) and 4.6 a) shows the carrier concentrations achieved using the lower doped P-Anode, with 4.5 b) and 4.6 b) showing the concentrations achieved using the higher doped P-Anode. Both the ion implant values demonstrate the achievement of conductivity modulation within the n-type drift region over and above the original donor doping concentration of $N_d = 3\text{E}15 \text{ cm}^{-3}$. The upper limit of the conductivity modulation level achieved within the drift region is set by when the injector itself becomes conductivity modulated (the anode in the case of hole injection, and substrate in the case of electron injection). Conductivity modulation occurs first in the lowest doped of the two injector conductivity types. For example, in the case of the ion implant anode doped to a peak of $N_a = 1.15\text{E}17 \text{ cm}^{-3}$ then this conductivity modulates first because the electron injector (substrate is doped to a higher level of $N_d = 1\text{E}19 \text{ cm}^{-3}$).

The gradient of carrier concentration at high levels of conductivity modulation is in line with the diffusion current from injector with the highest impurity doping concentration to lowest. In the case of the ion implanted anode with peak doping set at $1\text{E}20 \text{ cm}^{-3}$ then the electron injector (Substrate) achieved conductivity modulation first as this was the lowest doped of the two injectors.

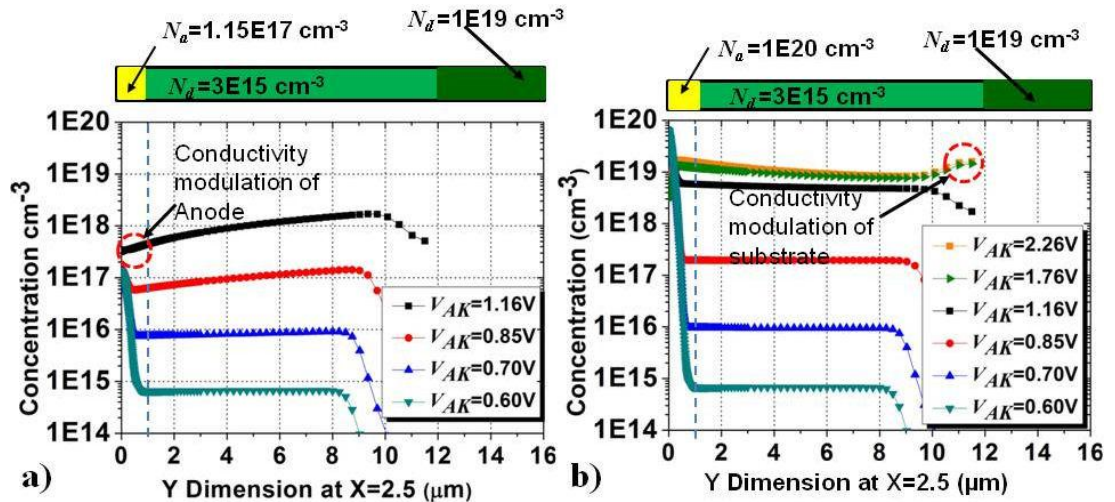


Figure 4.5. Hole concentration as a result of forward bias on a p-type region doped to a peak of a) $1.15\text{E}17 \text{ cm}^{-3}$, b) $1\text{E}20 \text{ cm}^{-3}$.

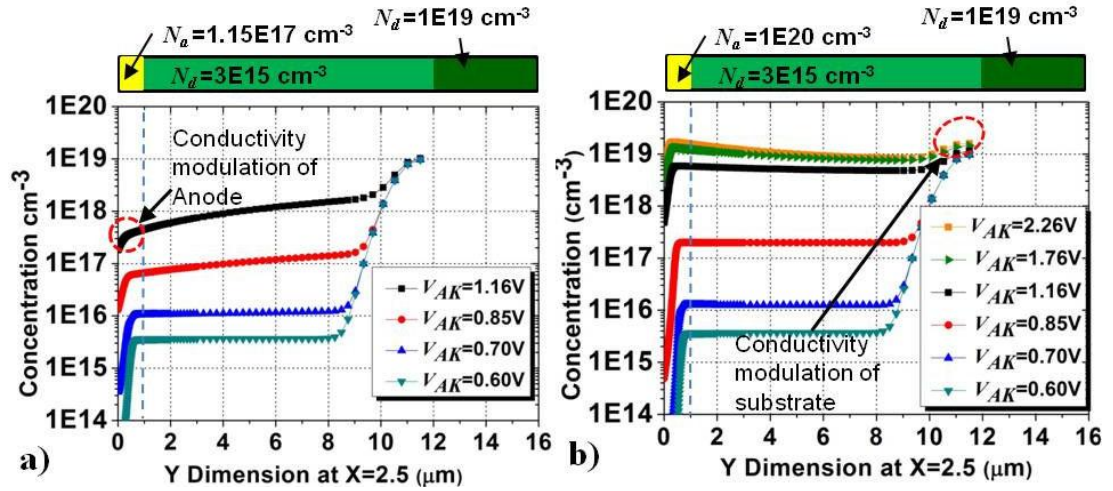


Figure 4.6. Electron concentration as a result of forward bias on a p-type region doped to a peak of a) $1.15\text{E}17\text{ cm}^{-3}$, b) $1\text{E}20\text{ cm}^{-3}$.

The effect of increasing temperature on a silicon P-N junction was described by Sze[2] as two-fold, wherein not only does the mobility fall with increasing temperature, but also the intrinsic carrier concentration (n_i) increases. The net result is that a reduction in the built in potential occurs with increased temperature (see equation A3.1.1) assisted by the increase in carrier concentration due to the upward shift in n_i (see equations 4.1, A3.1.4 and figure 3.26). For decreasing temperatures the converse applies.

4.2.2 Minority injection from a Schottky diode

A Schottky diode is made by contacting a metal to an n-type semiconductor, it is a unipolar device utilising electrons as the majority carrier. The device is attractive for use as a rectifier due to the low voltage drop across the junction (typically 0.3V in silicon) and fast switching times, due to unipolar operation, hence reduced power losses in both static and dynamic situations according to Baliga[6]. Devices are commercially available to a rating of 100 V, but SiC devices have now extended that range to compete with PiN diodes and yet have eliminated the large recovery currents associated with the silicon PiN structure. For rectifying applications it is normally desired to create a device with a low barrier height as represented in figure 4.7 where the metal work function (Φ_M) is as close to the electron affinity of silicon ($q\chi_{si}$) as possible (where $q\chi_{si} = 4.05\text{ eV}$). As is required to form an Ohmic contact for lowest on state loss and yet still enable an adequate potential barrier (Φ_{Bn}) to

function as a rectifier and therefore reducing the tunnelling current due to an extended depletion width. The work function provided by a selection of commonly used metals as provided within Synopsys Medici[5] is shown in table 4.1. As described by Rhoderick[7] the surface states generally dominate the actual barrier height achieved in practice. If the surface charge is negative the bands bend upwards and increase the barrier height from that expected from the metal work function used. In addition Rhoderick[7] also discussed the presence of a very thin layer (10-20 Angstroms) of silicon dioxide, the action of which is to increase the barrier height. The simulations used herein however, assume a perfect interface with no surface states. The field emission or tunnelling model (SBT) was activated within each Synopsys Medici simulation[5].

Metal	Metal work function, Φ_M (eV)
Aluminium (Al)	4.10
Tungsten (W)	4.63
Tungsten disilicide (WSi_2)	4.80
Titanium (Ti)	4.33
Titanium – Aluminium (Ti-Al)	4.51
Nickel disilicide (NiSi_2)	4.7

Table 4.1. Commonly used metal contacts and their associated work functions.

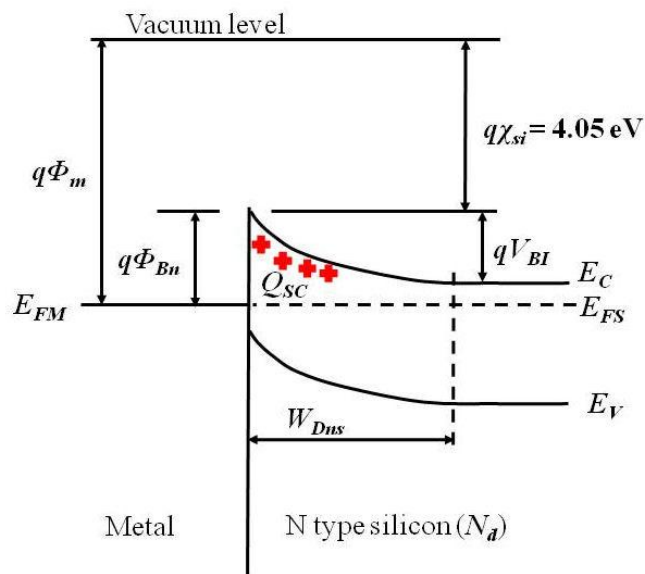


Figure 4.7. Band diagram at the interface between a metal and n type Silicon at thermal equilibrium.

Using the abrupt junction approximation the depletion width as a result of the metal to n type semiconductor contact is shown in equation 4.7.

$$W_{Dns} = \sqrt{\frac{2K_s \epsilon_o}{qN_d}} (V_{BI} - V_{AK}) \quad (\text{cm}) \quad (4.7)$$

The barrier height is reduced when the potential bias (V_{AK}) applied to the semiconductor side (cathode) is negative relative to the metal contact (anode). The barrier height lowering is known as the Schottky effect, or image force lowering, as described by Sze[2] and Rhoderick[7]. When adequately forward biased the Schottky device conducts current (electrons) at $V_{AK} = V_{BI}$. Within a low barrier height Schottky diode the current is predominately carried by the transport of electrons over the potential barrier by the thermionic emission process as described by Rhoderick[7] and possibly via field emission (quantum mechanical tunnelling) if the depletion layer width is relatively thin as in the case of a highly doped N-Drift region device. In the case of the intended injected VDMOSFET then the N-Drift region doping defined within chapter 3 was $N_d = 3 \times 10^{15} \text{ cm}^{-3}$. This relatively low epitaxial doping resulted in a relatively wide Schottky depletion layer width, which was preventative to tunnelling current. The total current density (J) across the Schottky barrier interface purely by the thermionic emission mechanism is as defined by Baliga[6] shown in equation 4.8.

$$J = A^* T^2 e^{-\left(\frac{q\Phi_{Bn}}{kT}\right)} \left[e^{\left(\frac{qV_{AK}}{kT}\right)} - 1 \right] \quad (\text{A/cm}^2) \quad (4.8)$$

Where A^* = the effective Richardson constant = $110 \text{ cm}^{-2} \text{ K}^{-2}$ for silicon.

According to Sze[2], the current density can be expressed in terms of the saturation current density (J_o) as follows:-

$$J = J_o \left[e^{\left(\frac{qV_{AK}}{\eta kT}\right)} - 1 \right] \quad (\text{A/cm}^2) \quad (4.9)$$

Where η = ideality factor related to the slope on the log/linear plot of I-V

If the N-Drift region is highly doped (for example $> 1 \times 10^{17} \text{ cm}^{-3}$) then field emission or ‘tunnelling’ may occur as the depletion width from the Schottky contact to N-Drift region

will be very thin. Electrons acquiring sufficient energy may therefore travel through thin the depletion layer associated with the Schottky junction. Pierret[4] describes the tunnelling carrier transport mechanism as only significant when the depletion width is $<10^{-6}$ cm. Tunnelling is predominantly associated with Ohmic contacts where the surface concentration is heavily doped thus ensuring a very thin ($<0.1\mu\text{m}$) metal to semiconductor Schottky depletion width which is effectively transparent to carriers.

The effect of varying the work function of the metal contact was evaluated by simulation of a Schottky with an otherwise fixed structure under identical ambient heat-sink conditions (at $T=300$ K) and calculation method. The $X=5\mu\text{m}$ wide model consisted of a $Y=10\mu\text{m}$ N-Drift region donor doped to $N_d=3\text{E}15\text{ cm}^{-3}$. A substrate of $N_d=1\text{E}19\text{ cm}^{-3}$ was also used to a total structure Y depth of $22\mu\text{m}$.

For the metal work functions with a relatively low barrier height ($\Phi_M < 4.7\text{ eV}$) the effect of increasing the work function on the resultant I-V characteristics can be seen in figure 4.8. With increasing levels of forward voltage (V_{AK}) the effect of changing the work function (Φ_M), hence barrier height (Φ_{Bn}) is to alter the V_{BI} level at which conduction begins via thermionic emission. A constant Ohmic slope is achieved subsequent to overcoming the barrier as provided by the N-Drift donor doping concentration, please see equations 4.2 and 4.4 earlier. As can be seen in figure 4.8 b), the work function also has a direct influence on the saturation current of the Schottky junction (J_O), wherein the saturation current falls rapidly with increased metal work function. With little or no tunnelling or depletion layer recombination then J_O is dictated by the thermionic emission current and η is close to unity according to Sze[2]. At low temperatures and/or increased N-Drift doping then tunnelling increases and both J_O and η increase, according to Sze. The I-V characteristics for Schottky diodes using work functions greater than $\Phi_M \geq 4.8\text{ eV}$, hence resulting in large barrier heights, are shown in figure 4.9.

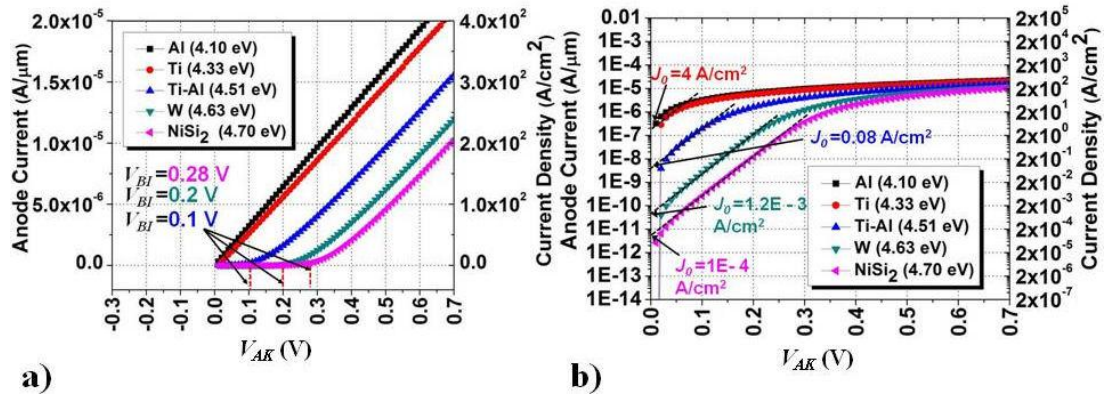


Figure 4.8. The effect of increasing the metal work function up to $\Phi_M=4.7$ eV on the forward Schottky diode characteristic using: a) linear Y scale, b) Log Y scale.

The calculations to check the built in potential of the Schottky (V_{BI}) as shown in figure 4.8 a) are shown at Appendix 4.3, The calculated V_{BI} for Tungsten (W) (at 0.35 V) however, was higher than the simulated result shown at $V_{BI} = 0.2$ V. This was due to the effects of field emission through the depletion region prior to the onset of thermionic field emission over the barrier as indicated by the gradient of the I-V characteristic. The 0.35 V as calculated corresponds only to the onset of thermionic field emission which as shown in figure 4.8 a) as the start of the linear part of the I-V characteristic due to the drift region resistance.

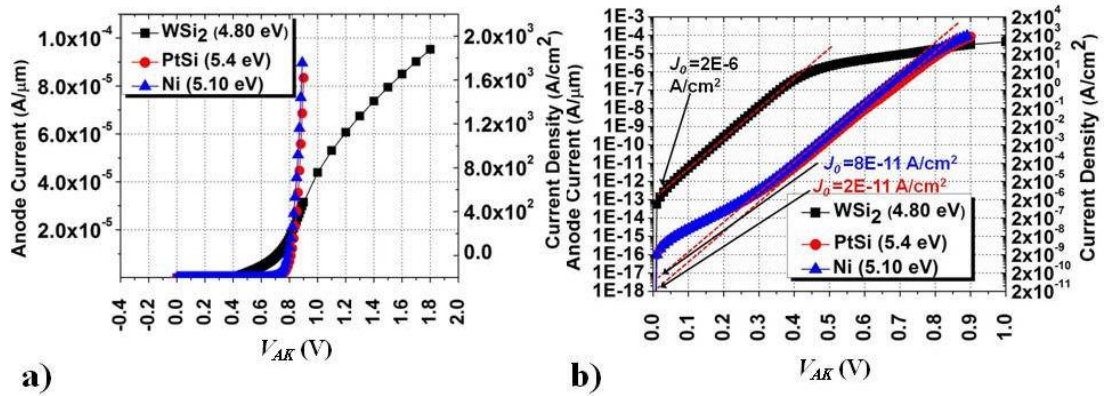


Figure 4.9. The effect of increasing the metal work function from $\Phi_M=4.8$ eV on the forward Schottky diode characteristic using a) linear Y axis, b) Log Y axis.

Clearly from figure 4.9 if the barrier height is made deliberately large where $\Phi_M=4.7$ eV, then the high barrier combined with a much reduced saturation current level (J_0) results in conductivity modulation of the drift region as first described and investigated

by Scharfetter[8] in 1963. Scharfetter used an injection ratio (γ_s) which described the ratio of current carried by majority carriers to that carried by minority carriers. The injection ratio was described as a function of the total current density as shown in equation 4.10. With increased current density, for a given barrier height and doping, then the ratio of minority carrier current to majority current were increased.

$$\gamma_s = \left[\frac{n_i}{N_d} \right]^2 \frac{J_n}{bJ_o} \quad (4.10)$$

Where factor $b = \mu_n/\mu_p$.

The injection ratio therefore is a method to compare the injected electron concentration in the N-Drift region to the resultant generated and stored holes which eventually form an excess which is available to recombine in the N+ substrate. A pictorial representation of the carrier concentration under a low current density scenario is shown in figure 4.10. In comparison the same Schottky diode is shown in figure 4.11 under high current density

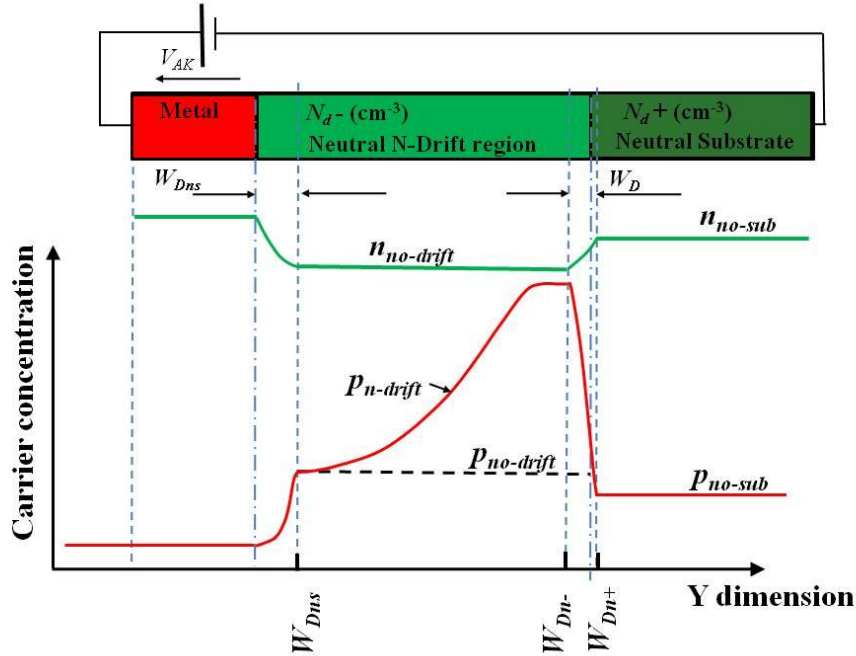


Figure 4.10. Carrier concentration within a Schottky diode at low current density (J_n).

conditions with increased injection ratio. Upon comparison of figure 4.9 with figure 4.10 the concentration of holes can be seen to grow with increased V_{AK} bias (and hence increased

current density as shown in figure 4.9), however the concentration level shown in figure 4.10 remains lower than the donor doping level within the N-Drift region and hence does not affect the I-V characteristic. However, if the current density is further increased then the injection ratio (γ_s) would increase due to charge storage within the N-Drift region.

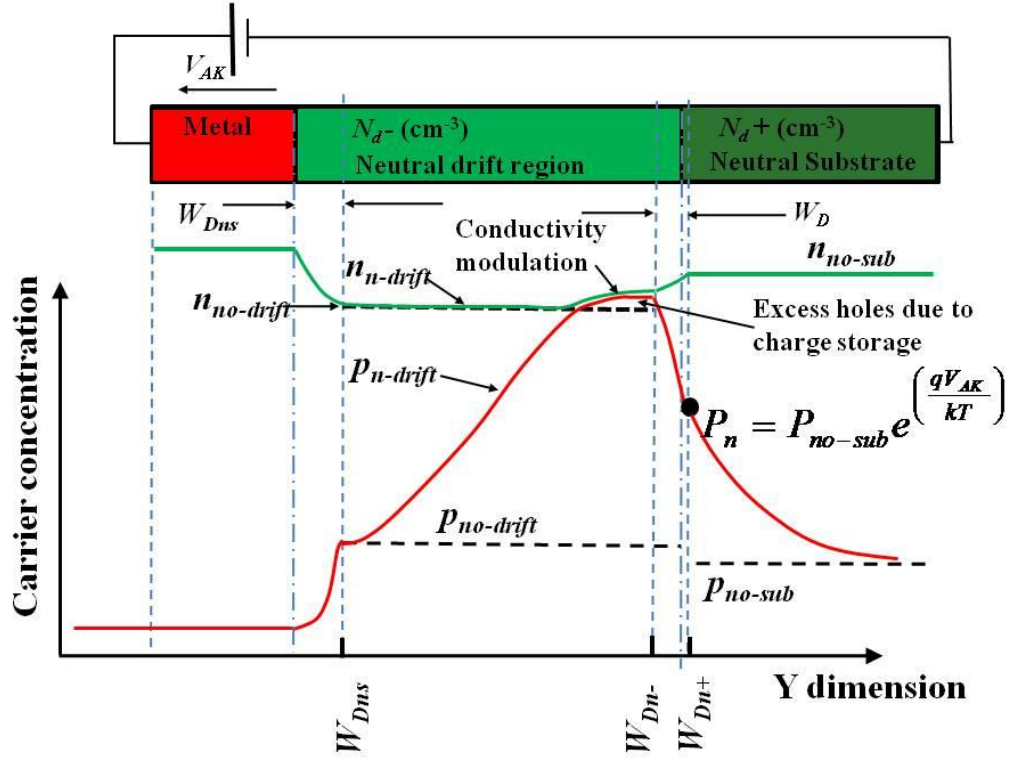


Figure 4.11. Carrier concentration within a Schottky diode at high current density (J_n).

The amount of stored charge (Q) in the N-Drift region of a Schottky according to Scharfetter[8] was the product of the current dependant attenuation length (the distance holes drift in a lifetime) and the minority carrier concentration at the semiconductor side of the Schottky contact space charge region (at W_{Dns}) as shown in equation 4.11.

$$Q = \left[\frac{n_i J_n}{N_d} \right]^2 \frac{\tau_p}{b J_0} \quad (4.11)$$

Where factor $b = \mu_n / \mu_p$, τ_p = lifetime of holes.

From equation 4.11 clearly at decreased saturation current levels (J_o), as achieved when using a high barrier height Schottky, then the amount of stored charge in a given volume would increase as given by the hole concentration, ($p_{no-drift} + p_n \text{ cm}^{-3}$) as shown in figure 4.11. Similarly, from equation 4.10 the use of a high barrier height Schottky contact with a low saturation current (J_o) would mean that conductivity modulation could occur within the N-Drift layer at much lower current densities (J_n).

The experimental work of Jager[9] confirmed that via the resultant saturation current density (J_o) an increased barrier height has a strong influence on the injection ratio and charge storage, hence on the level of conductivity modulation achieved. Another major factor was identified as the donor concentration of the N-Drift region, where higher donor densities required much higher current densities to obtain a high injection ratio in a low barrier Schottky. As regards charge storage the epitaxial thickness is also critical according to Scharfetter[8]. The distance holes traverse the N-Drift region at low current densities (low injection levels) is dictated by the minority carrier diffusion length as shown in equation 4.12.

$$L_p = \sqrt{D_p \tau_p} \quad (\text{s}) \quad (4.12)$$

Where D_p is the diffusion constant (in cm^2/s) for holes and τ_p is the carrier lifetime for holes). However, at increased current densities it is set by the distance holes drift in a lifetime according to Scharfetter[8] who went on to state this distance could become large as it increased linearly with forward current.

The issue with a high injection ratio (γ_s) was that the holes generated within the N-Drift region, to enable the electrons to transit through the N-Drift region and hence over the barrier, need to recombine to be removed from the N-Drift region at the junction to the N+ substrate. This junction therefore acts in a similar manner to a P-N junction where minority carriers recombine in the space charged region of width W_D with injected majority carriers, or within the substrate. Recombined electrons in the substrate are replaced via the substrate Ohmic contact, thus a net current flow occurs due to the excess holes. In a low barrier

height, highly doped thin N-Drift region (where for example $W_{Dns} < 1\mu\text{m}$, $D_L=2\mu\text{m}$) with low current density then minority carriers are not stored as the recombination rate at the N+ substrate to N-Drift junction is greater than the electron injection and subsequent hole generation rate. However, with increased current density then holes traverse further from the N+ substrate due to drift thus the injection rate and generation rate occur at a faster rate than the recombination's resulting in much more charge storage within the N-Drift region. In effect the holes become trapped within the N-Drift region. The effect of the stored holes is to alter the requirements to maintain charge neutrality where:-

$$p_n - n_n + N_d - N_a = 0 \quad (\text{cm}^{-3}) \quad (4.13)$$

As a result of an increase in p_n , then n_n must also increase simultaneously. The effect of the stored holes would be to slow down the switching of the Schottky with a high injection ratio according to Scharfetter[8], but in the case of the injected VDMOSFET hybrid device using a high injection ratio Schottky the hole storage issue is removed by the grounded P-body acting as a collector of holes.

The work of Chuang[10] in 1983 was to demonstrate the effect of using various thicknesses of N-Drift region with a high barrier height Schottky, this was created using a platinum silicide contact (PtSi). The effect of a thick N-Drift region was to greatly increase the charge storage capacity within a Schottky diode, as predicted by theory the minority charge storage time (hence the amount of charge stored at any one instant) increased with current density. The use of a PtSi contact as described by Ottaviani[11] who stated the work function of platinum to be 5.4 eV, the resulting metal-semiconductor junction provided a barrier height of 0.85 eV. The manufacture of self aligned PtSi contact was discussed by Zhang[12]. Through the use of a high work function metal such as platinum, or alternatively iridium silicide (IrSi), as described by Ohdomari[13], then a high barrier height device could be produced. As regards the use of nickel (Ni) then this metal has a work function of around 5.0 eV, thus could potentially provide a high barrier height Schottky, but the resultant barrier height can vary due to the various nickel silicide compounds that may be formed as a result

of process variation which can have widely differing work functions as reported by Biswas[14].

The resulting simulations of the carrier concentrations within a platinum silicide Schottky contact ($\Phi_M=5.4$ eV) are contrasted with those of a tungsten contact ($\Phi_M=4.63$ eV) and tungsten disilicide ($\Phi_M=4.8$ eV) as shown below in figures 4.12 and 4.13 for electrons and holes respectively. The resultant electric field is shown in figure 4.14 using the identical Y dimension scale. Through comparison of figure 4.13 with figure 4.14

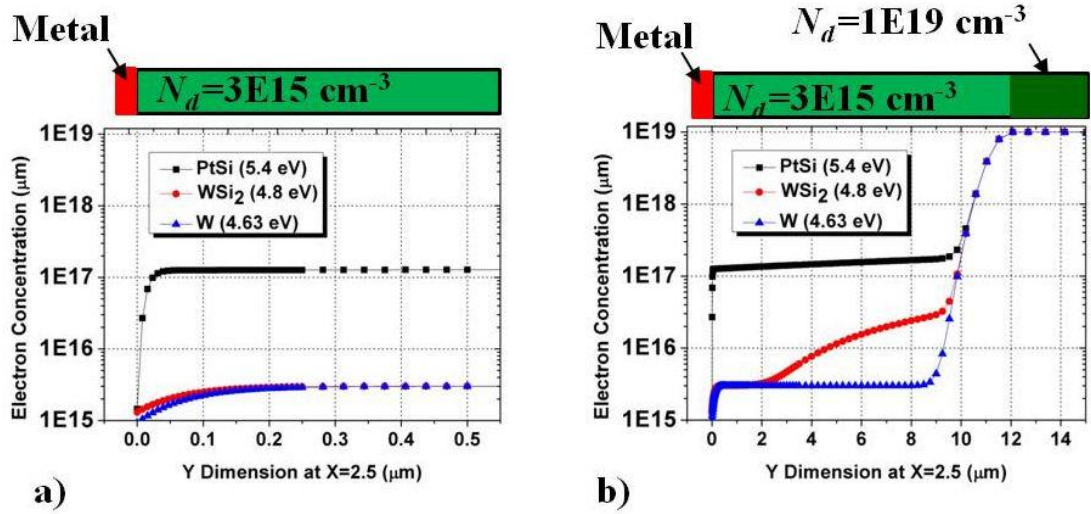


Figure 4.12. Electron concentration at $V_{AK}=0.85$ V across a modelled one dimensional Schottky diode: a) zoom to contact, b) throughout N-Drift region to substrate.

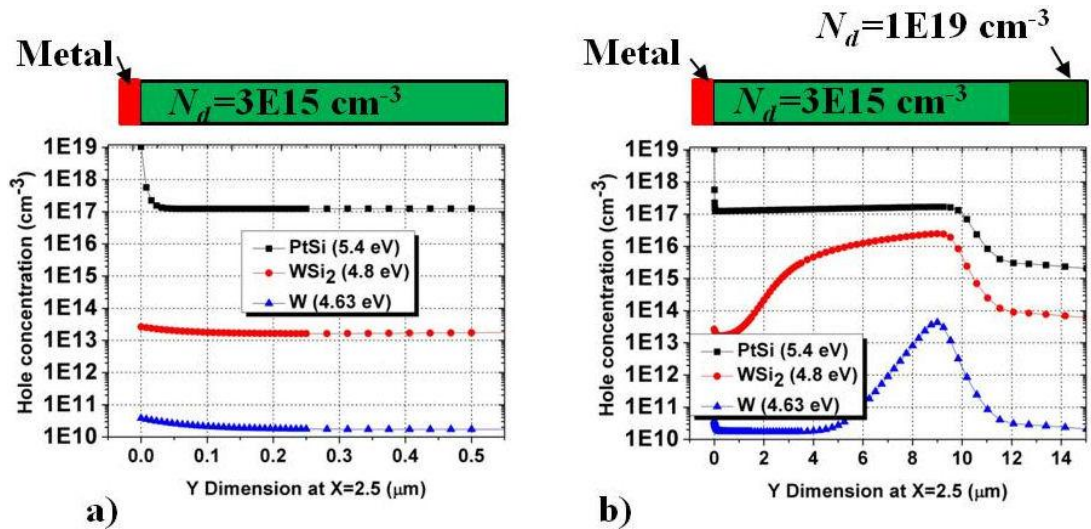


Figure 4.13. Hole concentration at $V_{AK}=0.85$ V across a modelled one dimensional Schottky diode: a) zoom to contact, b) throughout N-Drift region to substrate.

then the peak hole concentration occurred at the extent of the depletion from into the N-Drift region from the junction with the N⁺ substrate at Y=9 μm , this was in agreement with theory as depicted in figure 4.10 and 4.11. The extent of the hole storage displayed in figure 4.13 towards the Schottky contact was dependent upon the barrier height of the metal used,

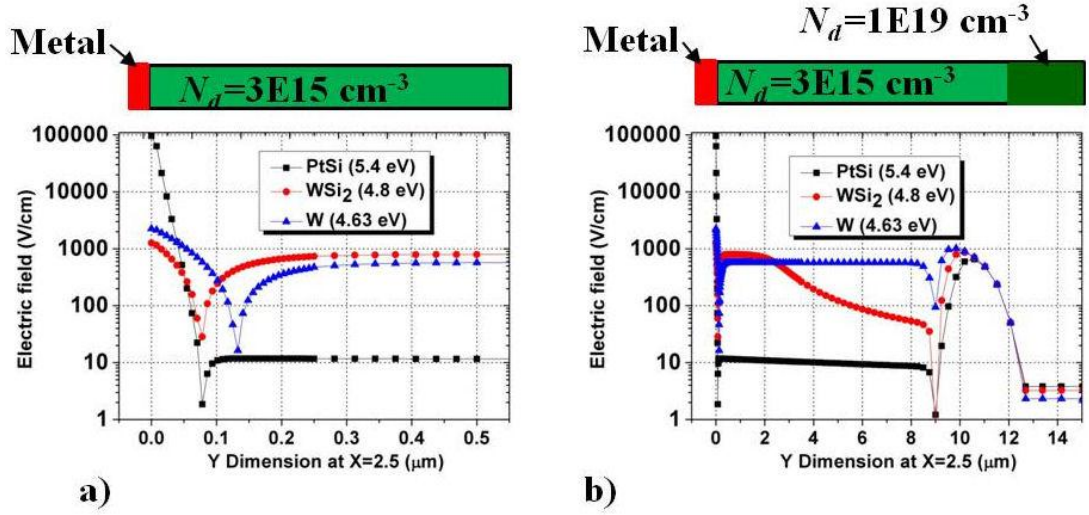


Figure 4.14. Electric field at $V_{AK}=0.85$ V across a modelled one dimensional Schottky diode: a) zoom to contact, b) throughout N-Drift region to substrate.

again as agreed through theory. By comparison of the depletion widths of the various metals used to form the Schottky contacts as shown in figure 4.14 then at $V_{AK}=0.85$ V the high barrier height PtSi contact provided a very high, but narrow depletion, thus enabling a large tunnelling current to flow when conductivity modulated. The progression of the electric field depletion width from the Schottky junction in to the N-Drift region with bias level (V_{AK}) for the PtSi device is shown in figure 4.15. As can be seen in figure 4.15 a) the depletion region reduces progressively with increased bias introducing an increased level of tunnelling current. Eventually very high electron drift and diffusion current densities are allowed to flow via the tunnelling mechanism this fact overcomes the otherwise adverse effects of the subsequent increase in saturation current density (J_0) (rising with tunnel current) and increase in N-Drift doping concentration (N_d), as indicated by equations 4.10 and 4.11.

The effect of low and high barrier height Schottky contacts on the minority carriers within the N-Drift region was investigated and measured by Wagner[15] through simulation

and measurement of the quasi Fermi potential for holes (QFP). As described by Wagner the quasi Fermi potential for holes (QFP) and electrons (QFN) indicate the voltages within the

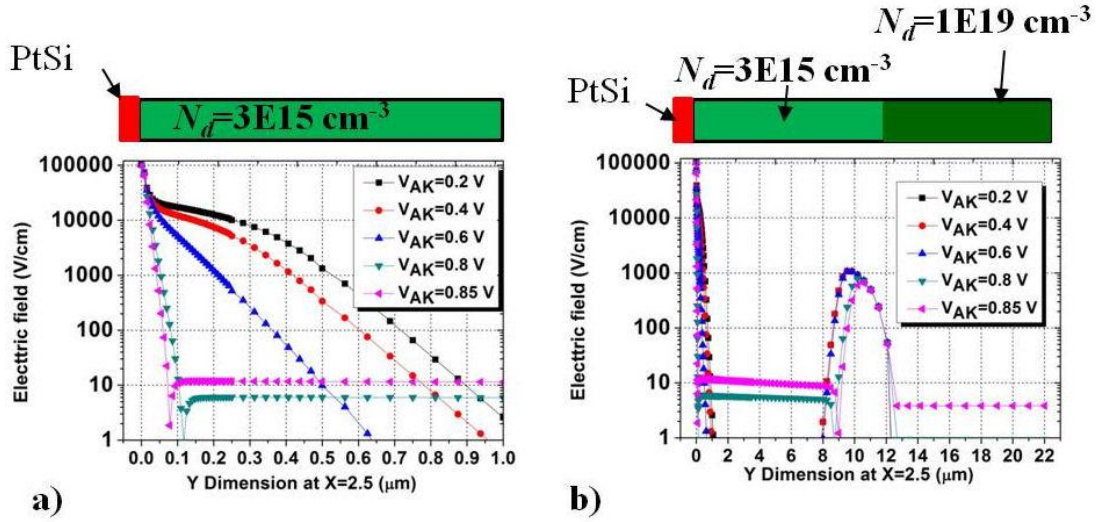


Figure 4.15. Electric field as a function of bias across a modelled one dimensional PtSi Schottky diode: a) zoom to contact, b) throughout N-Drift layer to substrate.

Schottky diode acting upon the carriers. Comparative plots of the Quasi Fermi potential for both electrons (QFN) and holes (QFP) are shown in figure 4.16 a) and b) respectively for the Schottky diode structure simulated with differing Schottky contact metal work functions. The QFN and QFP results for PtSi and W contacts shown in figure 4.16 are in stark contrast

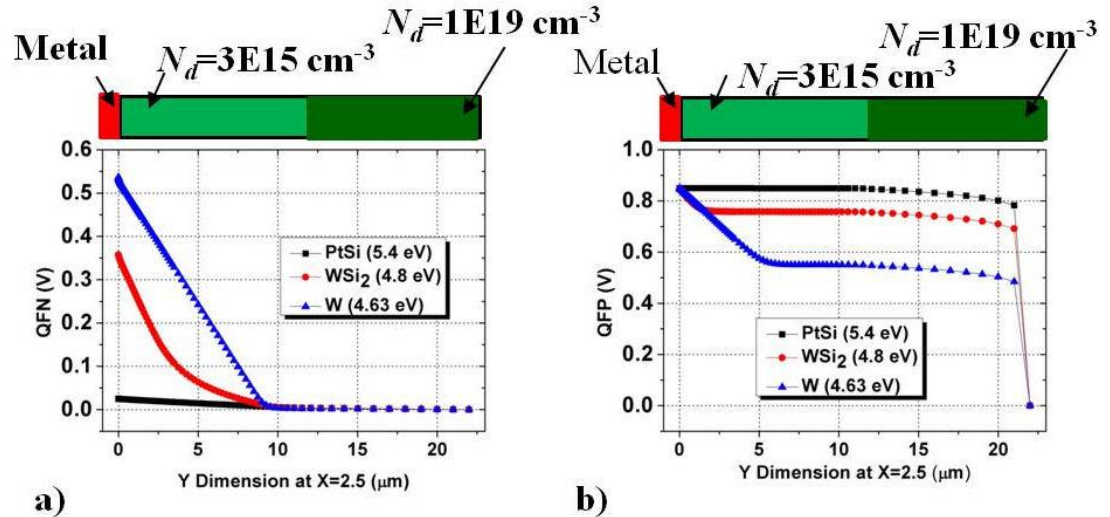


Figure 4.16. Quasi Fermi levels at $V_{AK}=0.85\text{V}$ throughout a modelled one dimensional Schottky diode: a) QFN, b) QFP.

to those of the tungsten disilicide (WSi₂) contact due to the change in the carrier concentrations, as shown in figures 4.12 and 4.13. The slope in the QFN or QFP plots of

figure 4.16 indicates the space charge region where carriers drift under the influence of an electric field, the field in turn is due to the charge. The current is very low in the PtSi Schottky diode due to the very low saturation current level (J_0) however; the storage of holes is very high as indicated by the constant QFP. As a result of the conductivity modulation, the resistance of the PtSi structure is very low; hence the slope of the QFN plot is also very low in figure 4.16, whereas the relatively high slope of QFN and QFP for tungsten indicates the highest resistance structure. At a bias level of 0.85 V the resistivity values of the Schottky diodes formed from the tungsten and platinum silicide contacts are calculated by substitution of the achieved carrier concentration (N_d) into equations 4.2 and 4.3 respectively.

4.2.3 Minority injection within a Junction Barrier Schottky diode

A Junction Barrier Schottky (JBS) diode is effectively a hybrid of a P-N junction and a relatively low barrier height Schottky. The device type was first described as a pinch rectifier by Baliga[16] in 1984 as fabricated in Silicon and described by Mehrotra[17]. Although, originally demonstrated in silicon, according to Zetterling[18] the JBS diode has found a niche when fabricated within silicon carbide (SiC). The aim of this device is to provide some conduction via the low barrier height Schottky (with $V_{AK} \approx 0.3$ V in silicon) prior to achieving forward bias of the P-N junction (with $V_{AK} \approx 0.7$ V in silicon). Thus, the forward conduction loss of the diode was reduced. The major benefit of the JBS diode was that it would provide a reduced reverse leakage current in comparison to a low work function Schottky diode (as caused by barrier height lowering, see Baliga[6]). The reverse breakdown voltage (BV_R) of the JBS diode is comparable to that of a P-N junction diode and hence overcomes the limitations of the Schottky barrier (which in silicon is limited to about 100 V typically in commercial devices as described by Baliga[6]). This is achieved through use of the depletion region extent from adjacent P type implants which when spaced correctly effectively shield the Schottky junction when the device is reverse biased according to Ivanov [19] , as shown in figure 4.17.

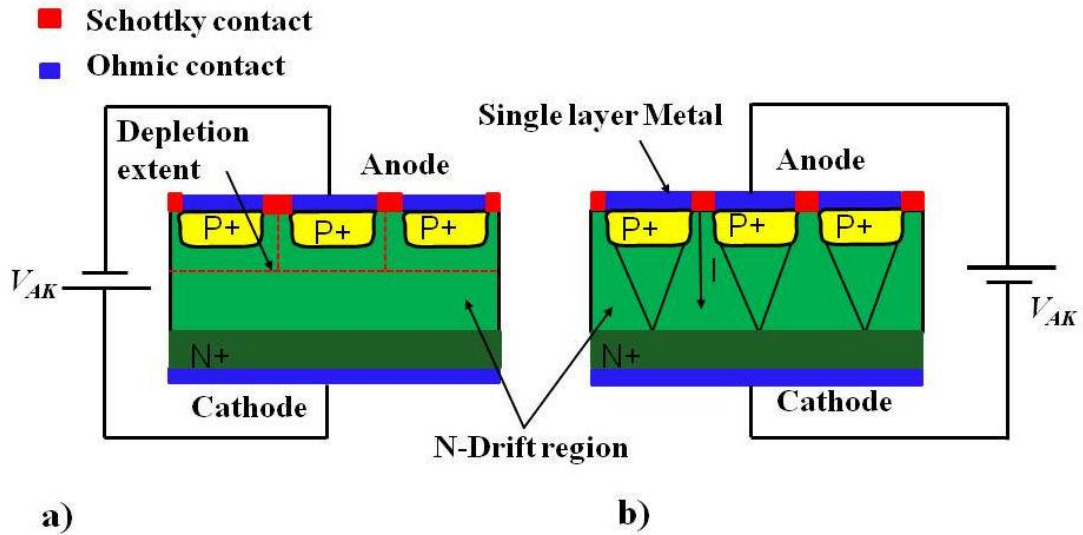


Figure 4.17. JBS diode in a) reverse blocking and b) forward conduction.

In terms of forward conduction, a silicon PiN rectifier, a silicon carbide Schottky and a silicon carbide JBS diode were compared over temperature by Millán[20] (with all devices rated to 1.2 kV). The JBS diode used within the work of Millán used nickel contacts as described by Brosselard[21]. Millán reported that in addition to the low forward volt-drop Schottky conduction start up (which reduced as temperature increased), the SiC JBS diode in forward conduction achieved bipolar conduction at current densities above 255 A/cm^2 when temperatures were $\geq 25^\circ\text{C}$, this led to a negative temperature coefficient in which the forward volt drop decreased with temperature. The resulting volt-drop within the SiC JBS diode was approximately 1 V lower at 300°C than the SiC Schottky device for twice the conducted current level. Below 25°C and up to 100°C however, it was stated by Millán that the bipolar conduction mode was not activated within the current limitations of the test set up, resulting in conduction only via the Schottky element within the JBS diode which had a positive temperature coefficient, therefore higher volt drop for a given current level. This was explained by the fact that the energy gap between the Fermi level and the intrinsic energy levels reduce, as a result the built in potential fell with increasing temperature. Thus within a P-N junction any increase in temperature will enable a lower V_{BI} and hence forward conduction.

As regards the potential use of the JBS diode injector concept within silicon, then it was envisaged that similar to the operation of the SiC JBS diode at lower temperatures described by Millán, then possibly a high work function Schottky element such as a PtSi contact would enable an increased voltage to be developed across the P-N junction and may enable lower temperature bipolar operation within the silicon device dependent upon the relative change in V_{BI} with temperature between the two junction types. However, the start up conduction voltage of the Schottky element (V_{FS}) with a high barrier height contact would increase and hence represent an increase in on state conduction loss which would not be desired in rectifying applications, but that did not limit the idea for use as a self biased minority carrier injector as IGBT devices typically began conducting at $V_{AK} \geq 1$ V.

4.2.4 Minority injection from an accumulation region of a MOS gate

The idea of using a Metal Oxide Semiconductor (MOS) inversion layer as a minority carrier injector (using Inversion Layer Injection, ILI) was discussed by Udrea[22]. The idea was extended by Udrea[23] for use within an Inversion Layer Injected Diode (ILID) and Inversion Layer Bipolar Transistor (ILBT). The resultant lateral, three terminal, ILBT device was constructed on an N-substrate on to which was grown a P-Drift region and utilised a P+ diffusion within an N-well. The gate electrode was extended out to overlap the N-well as shown in figure 4.18 a). The resultant device formed an electron channel and accumulation region under the gate when sufficient positive bias was applied to it relative to the cathode (V_{GK}) which extended to the N-well. Hence, sufficient electron charge was made available to forward bias the P-Anode to N-well junction to form a lateral IGBT.

In order to overcome the turn-off issues of the ILBT, then Udrea[24] proposed a double gated device called the Double Gate Lateral Inversion Layer Emitter Transistor (DGLILET) as shown in figure 4.18 b). In order to attract holes to a gate within an N-well then a negative bias would be required. The effect of the negative bias would be to accumulate holes at the surface just below the oxide. This occurred in a similar manner to that described in section 3 for the enhancement N-channel MOS gate structure, but the polarities are

reversed. In accumulation mode then the resultant hole charge from a strong inversion effectively forms an extended anode region from the P-Anode. Although the DG LILET had two gate controls of opposite polarity the device could still enter a latched Thyristor mode of operation and yet the complexity had doubled.

The same idea as used for the N-well ILI within the DG LILET could be used to form a floating P-Anode, dynamically controlled via a negative gate potential. The resultant floating P-Anode could possibly be resistively biased to inject minority carriers into the N-Drift region, where the potential developed across it was dependent upon the gate length and the electron current density flowing along that length. Unfortunately, the use of a negative bias with respect to ground added an unwelcome degree of complexity to the use of the device, as reliability is inversely proportional to complexity then this would cause additional reliability concerns. In addition as the P-Anode would float then it may be unpredictable as to when the injection start up may occur in terms of V_{AK} bias. The thin accumulation layer may also deplete at low bias levels and cause premature saturation of the I-V characteristic. Due to the above reasons further investigation work was not completed on this possibility, instead the work direction favoured the use of an implanted P-Anode with an Ohmic contact, rather than a temporary MOS gated P-Anode.

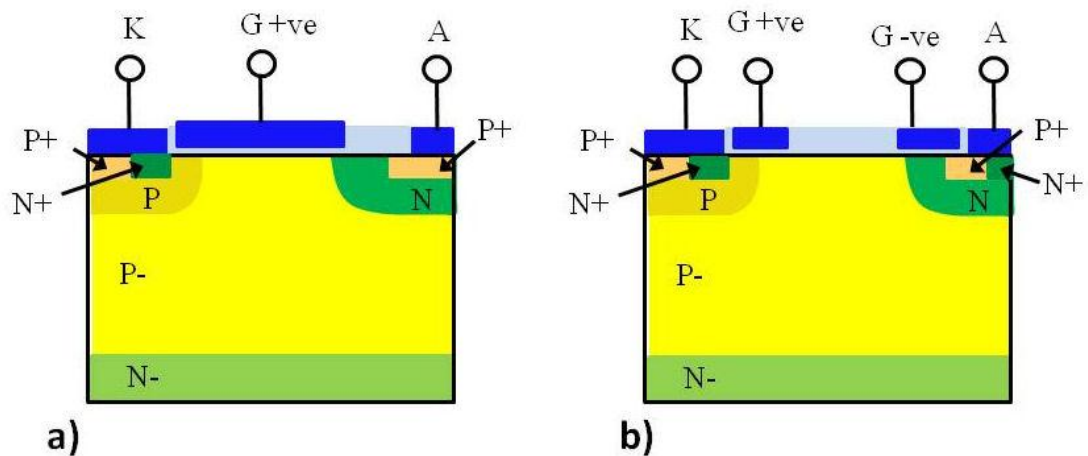


Figure 4.18. Examples of Inversion layer injection (ILI): a) Inversion Layer Bipolar Transistor (ILBT); b) Double Gate Lateral Inversion Layer Emitter Transistor (DG LILET).

4.3 Operation of the JBS type minority carrier injector

As a result of the comparison of minority carrier injector structures described within section 4.2 there was a possibility that a merged Schottky P-Anode structure such as that used within a JBS diode type minority carrier injector may provide benefits over a simple resistively biased P-Anode minority carrier injector structure when integrated in silicon within a VDMOSFET type structure. The operation of the JBS diode was therefore analysed through simulation to assess suitability. To complete the analysis of the JBS type minority carrier injector then two structures were simulated as shown in figure 4.19 a) and b). One utilised the N-Drift region contacted directly with an Ohmic contact as shown in figure 4.19 a), the other structure as shown in figure 4.19 b) used a substrate doped to $N_d = 1 \text{E}19 \text{ cm}^{-3}$. The key difference was the recombination rate of excess holes at a given temperature within the substrate as summarised by Pierret[25]:-

$$\left. \frac{\partial p_n}{\partial t} \right|_R = -\frac{\Delta p_n}{\tau_p} \quad (4.14)$$

Where:-

$$\tau_p = \frac{1}{c_p N_T} \quad (4.15)$$

Where c_p = capture coefficient of holes, N_T = number of recombination centres.

At an Ohmic contact then all carriers must immediately recombine due to the availability of an infinite number of recombination centres, whereas when a substrate is used then a fixed recombination rate will exist at any given temperature. This finite recombination rate effectively leads to an exponential decay in the concentration of excess holes within the substrate as the Y dimension is traversed. Majority carriers that recombine with minority carriers within the substrate are effectively replaced via the cathode Ohmic contact.

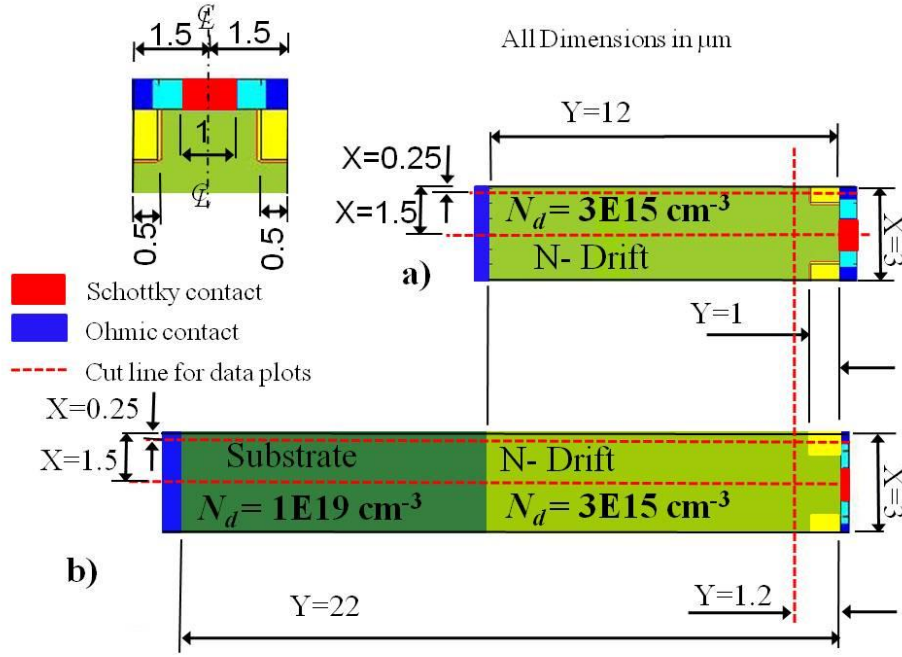


Figure 4.19. The as simulated JBS diode structures:- a) with no substrate, and b) with substrate.

4.3.1 Effect of substrate on JBS diode performance

The effect of the substrate on the hole concentration within the N-Drift region of the two modelled comparison JBS diode structures as shown in figures 4.19 a) and 4.19 b), both with a Schottky contact metal work function of $\Phi_M = 4.63 \text{ eV}$, is shown in figure 4.20 a) and 4.20 b) respectively. In turn the effect of the hole storage on the associated I-V characteristics of the two JBS diode types is shown in figure 4.21 a) and b) respectively. On comparison of figure 4.20 a) with 4.21 a) then the effect of the ideal recombination centre at the cathode Ohmic contact reduces the amount of hole storage to the extent where even at bias voltages $>$ the P-Anode to N-Drift layer junction forward bias point the hole storage is less than the donor doped side ($p_n < n_d$). However, the effect of hole storage within the N-Drift region due to the substrate has a clear impact on the start up voltage (V_i) at which the P-Anode to N-Drift junction becomes forward biased. This difference in P-Anode injection start up voltage (V_i) can be investigated through examination of the potential drop throughout the length of each structure as shown in figure 4.22, this however ignores any potential losses in the degenerate doped semiconductor.

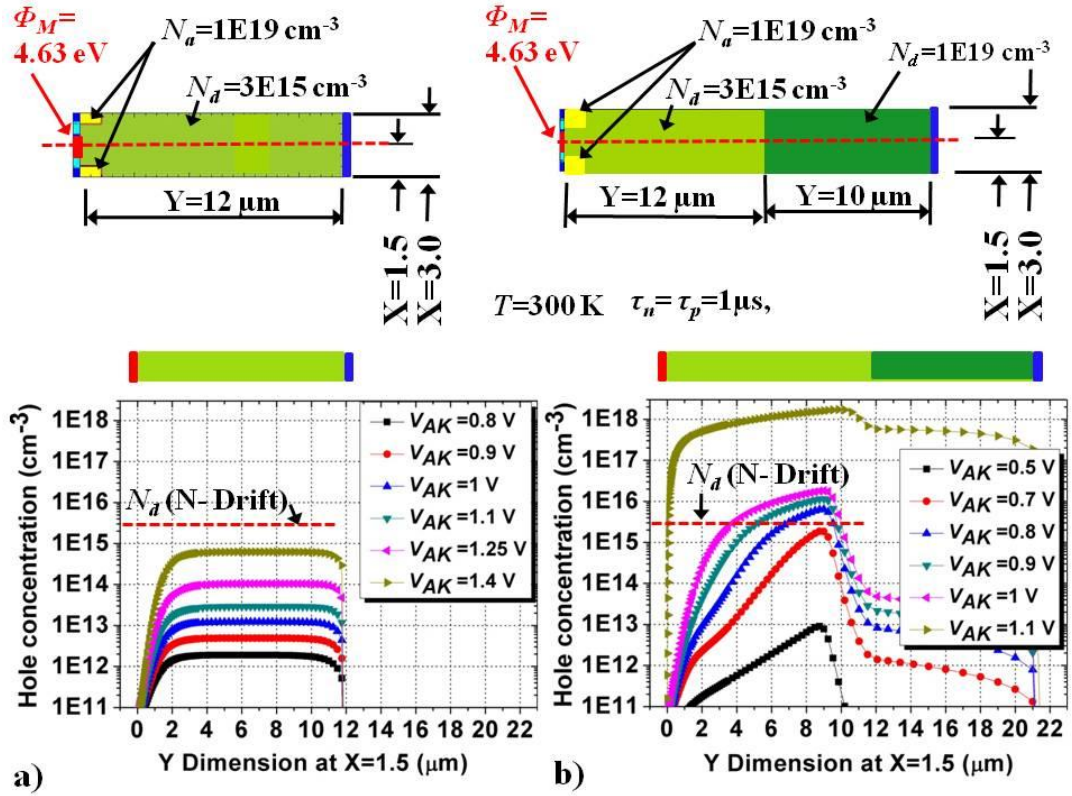


Figure 4.20. Hole storage within a JBS diode with $\Phi_M=4.63$ eV a): without and b) with substrate.

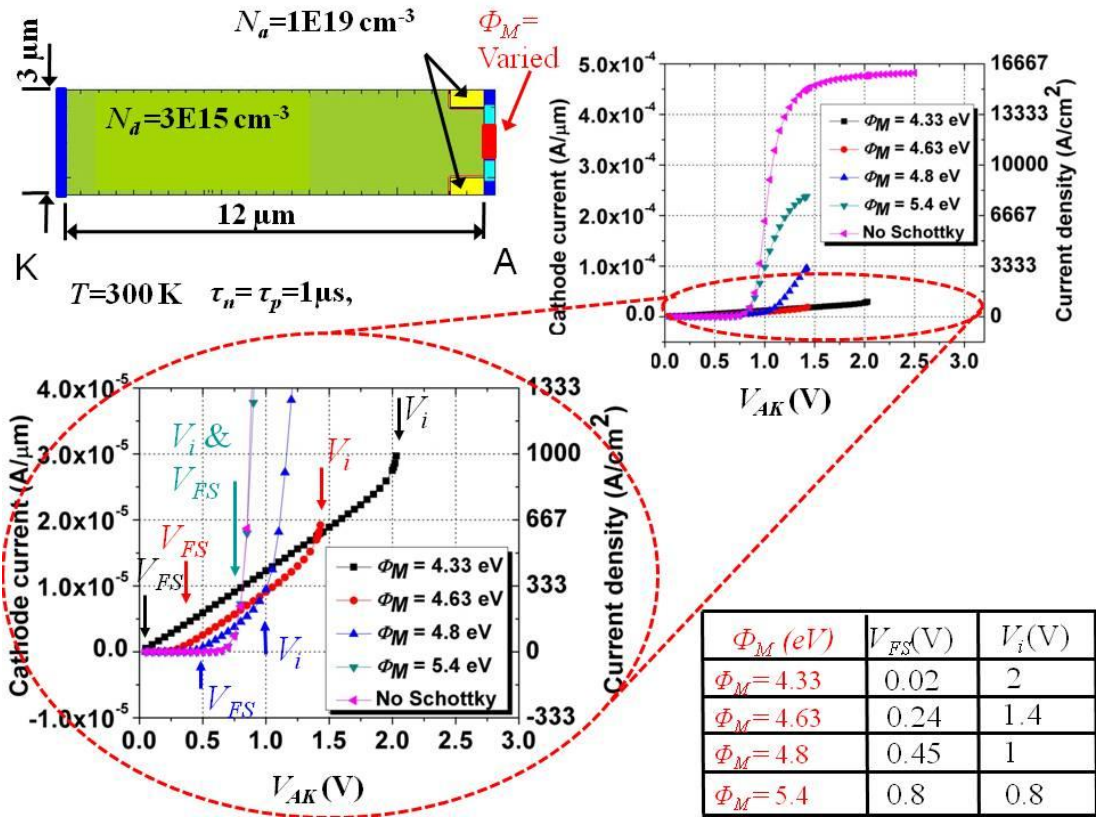


Figure 4.21 a). Forward I-V characteristics of JBS diodes without a substrate as the Schottky work function (Φ_M) is varied.

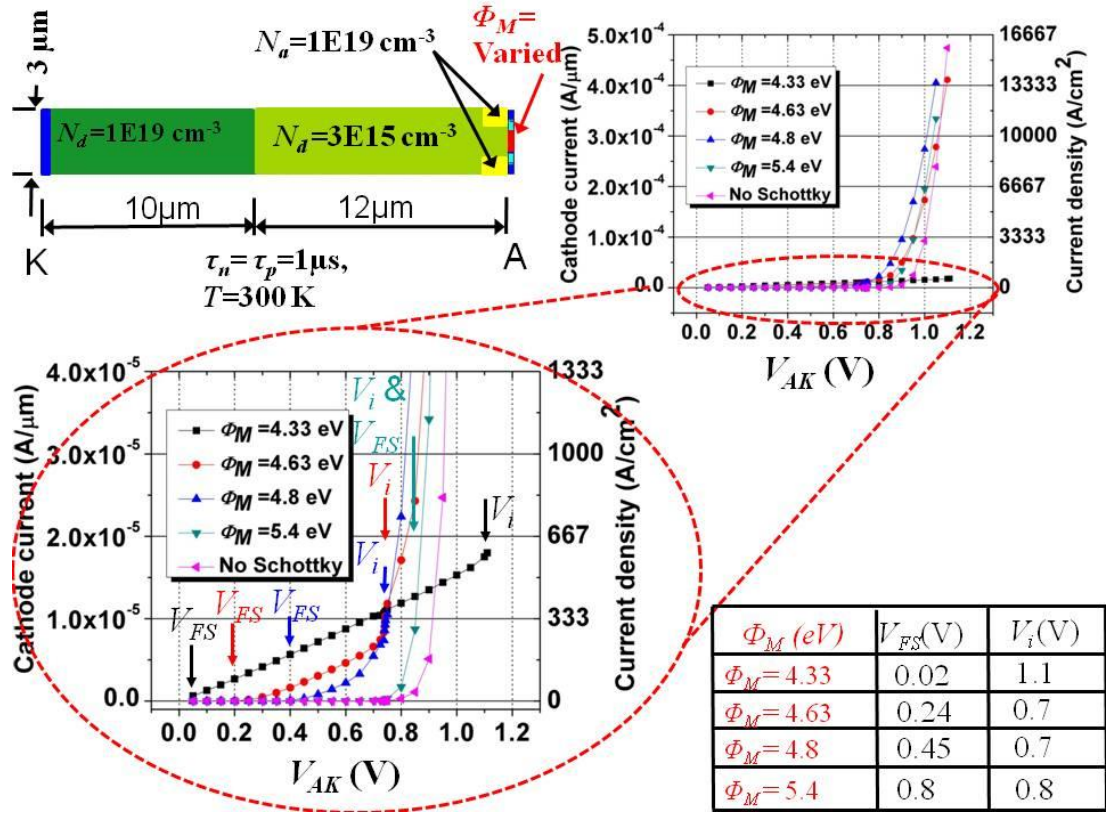


Figure 4.21 b). Forward I-V characteristics of JBS diodes with a substrate as the Schottky work function (Φ_M) is varied.

The structure shown in figure 4.22 is similar to that of a PiN diode, wherein the voltage drop across the P-Anode to N-Drift junction ($V_{P+ \text{ to } N-}$) can be calculated as a result of the hole concentration within the N-Drift layer (p_n) through use of equation 4.16.

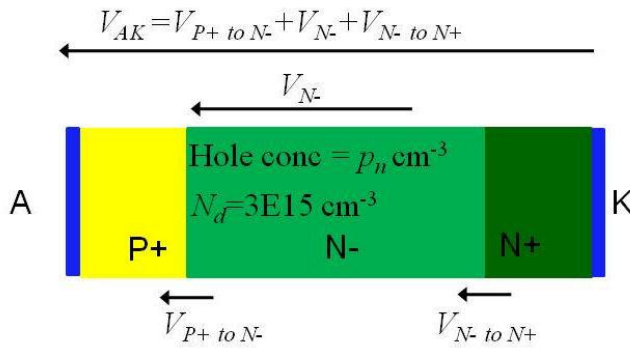


Figure 4.22. Generalised PiN diode doping structure and resultant accumulative potential.

$$V_{P+ \text{ to } N-} = \frac{kT}{q} \ln \left[\frac{P_n N_d}{n_i^2} \right] \quad (\text{V}) \quad (4.16)$$

Within a conventional PiN diode minority carrier injection would only occur from the P-Anode in accordance with equation 4.17 shown below.

$$p_n = p_{no} e^{\left(\frac{qV_{P+toN-}}{kT} \right)} \quad (V) \quad (4.17)$$

However, in the case of the JBS diode, which includes a Schottky junction, then as shown in figure 4.20 the intrinsic minority carrier concentration had already increased from ($p_{no} = 3.1E4 \text{ cm}^{-3}$) due to the storage of holes within the N-Drift region adjacent at the P-Anode junction, the stored charge from which can be calculated using equation 4.11. The effect is to reduce the P-Anode forward bias voltage from the value shown in figure 4.3 (0.93 V, for $N_a = 1E19 \text{ cm}^{-3}$), indeed the hole concentration p_n becomes the dominant effect in setting the voltage at which the P-Anode becomes forward biased (when $V_{AK} = V_i$) via the potential (V_{P+toN-}).

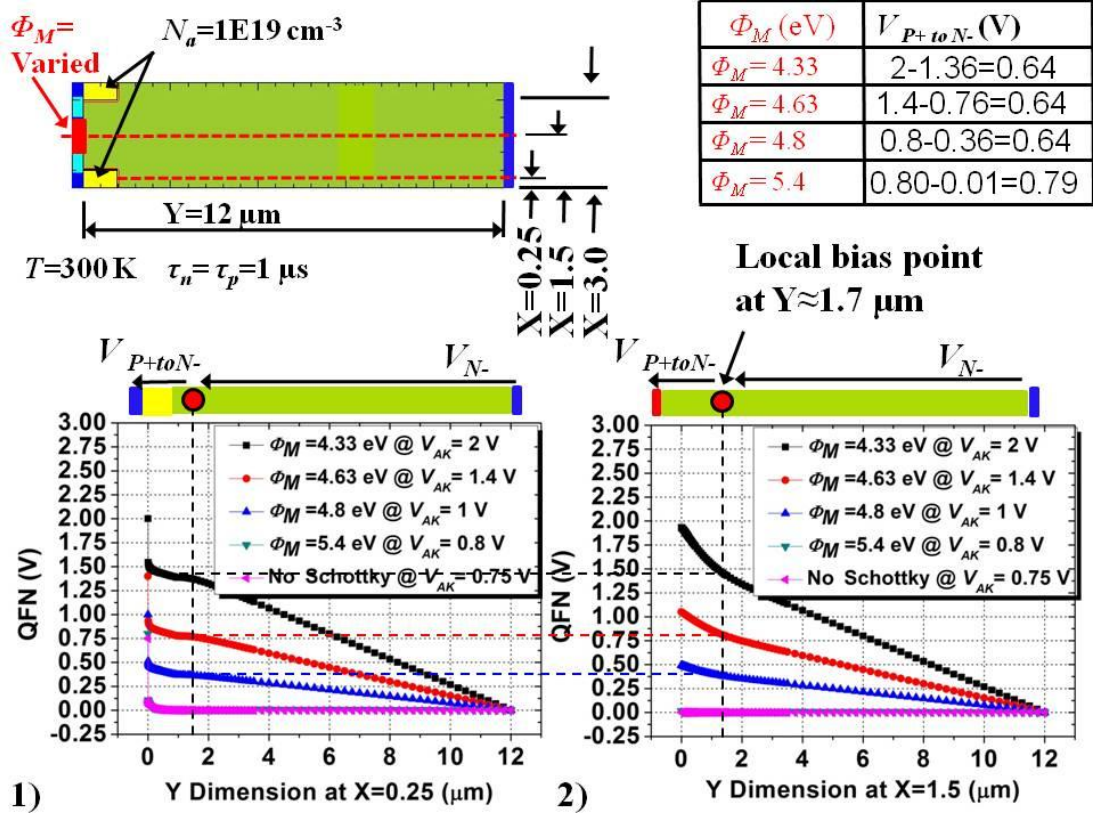


Figure 4.23 a). Electron Quasi Fermi potential of electrons (QFN) in a JBS structure without a substrate as the Schottky work function (Φ_M) is varied.

As V_{AK} is increased the potential developed within the structures when taken longitudinally as a cut at $X=0.25 \mu\text{m}$ through the P-Anode and $X=1.5 \mu\text{m}$ through the Schottky contact are shown in the form of plots of the Quasi Fermi potential for electrons (QFN, in units of V) against distance along the Y dimension line. The QFN plots for the JBS structures modelled without and with a substrate are shown in figures 4.23 a) and 4.23 b) respectively. The forward bias potential of the P-Anode to N-Drift junction is set at a local bias point which in turn is positioned at the furthest extent of the resultant depletion region from either the Schottky or the P-Anode, whichever is the larger width of the two. The local bias point therefore moves towards the P-Anode and Schottky as the level of hole storage increases. The remaining potential is dropped across the N-Drift region with a

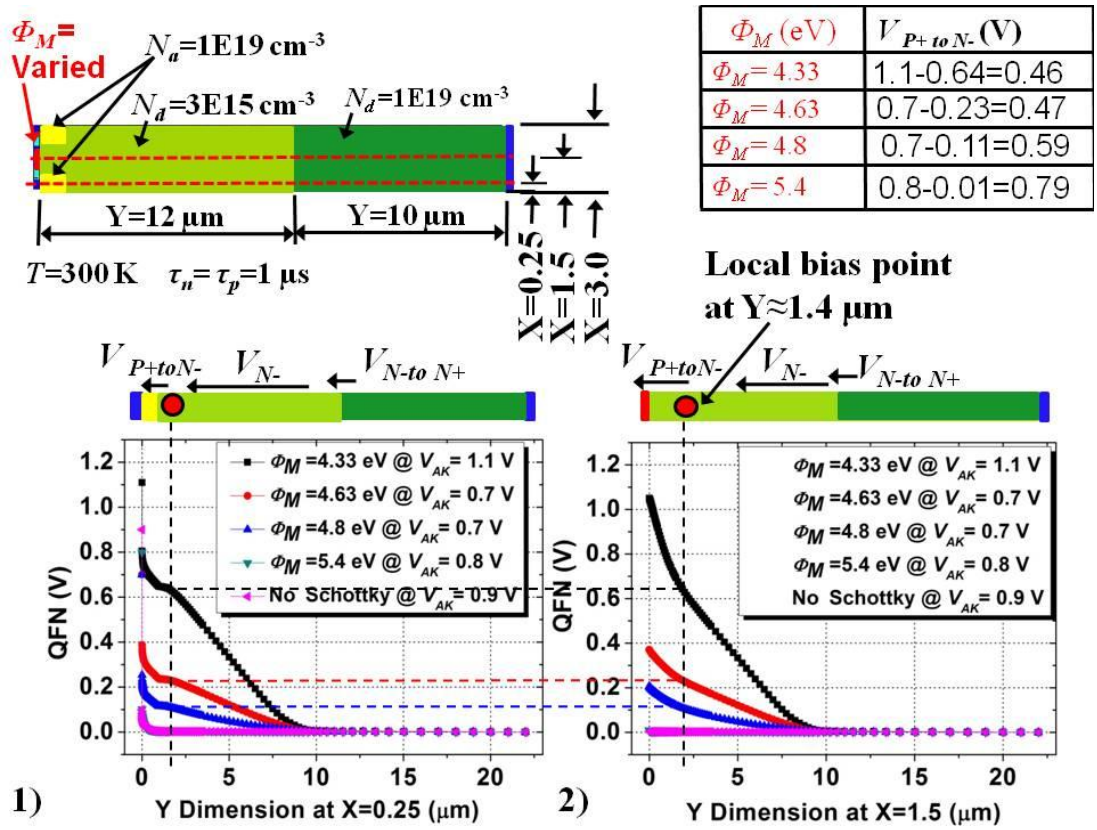


Figure 4.23 b). Quasi Fermi potential of electrons (QFN) in a JBS structure with a substrate as the Schottky work function (Φ_M) is varied.

small percentage dropped across the N+ substrate to N-Drift junction if one is present. As can be seen by comparison of figure 4.23 a) and 4.23 b) then the level of potential dropped

across the N-Drift region is again dependent upon the Schottky contact work function (Φ_M) used and the resultant hole storage.

The equivalent circuits of the structure without a substrate, and with a substrate, are shown in figure 4.24 a) and b) respectively. The predominant affect is the potential barrier to holes caused by the N+ to N- junction when the substrate is incorporated into the structure; this greatly increases the storage of holes within the N-Drift region as shown in figure 4.24.

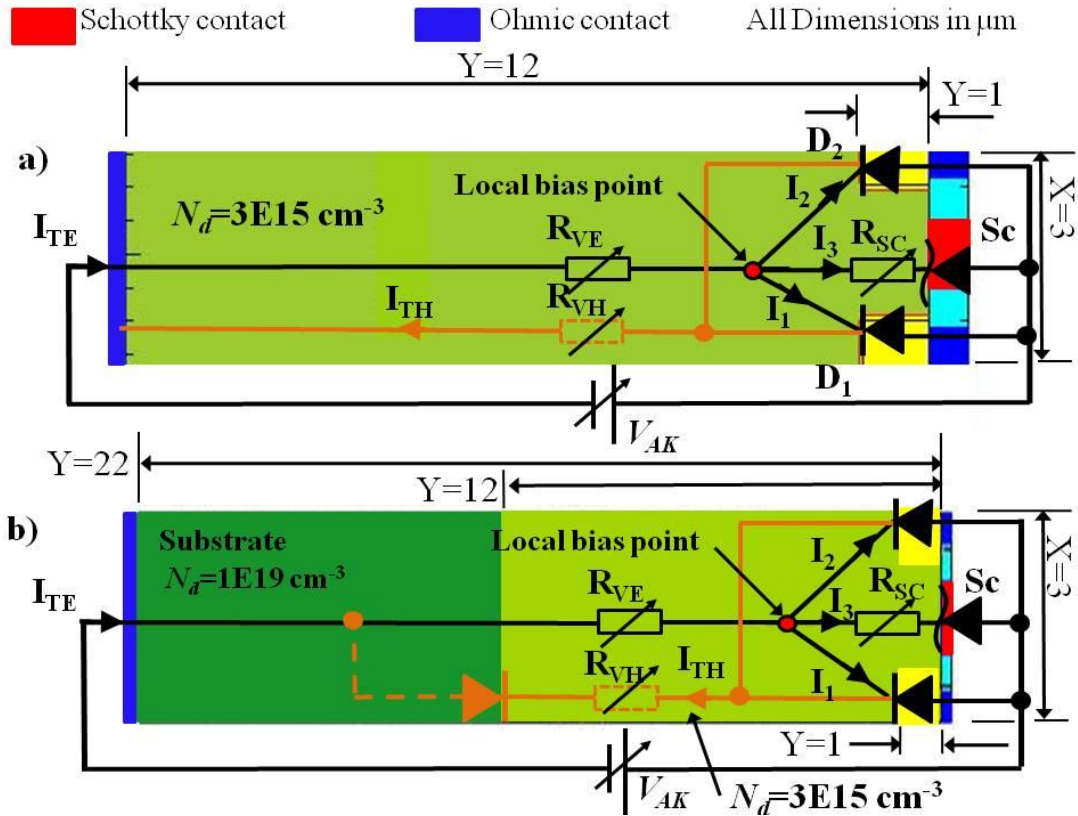


Figure 4.24. Effect of substrate on the equivalent circuit of a JBS diode a) without a substrate b) with a substrate.

4.3.2 Effect of Schottky work function on P-Anode bias

The effect of Schottky work function as discussed earlier directly affects the voltage $V_{P+ to N-}$ via the resultant hole storage, the remainder of the potential from the V_{AK} bias level is dropped across the N-Drift region again, this potential varies with the level of hole storage and hence the level of conductivity modulation. As can be seen from figure 4.23 a) and 4.23 b) the lowest work function of $\Phi_M=4.33$ eV results in the lowest level of hole storage and hence the voltage V_N is high, conversely the highest work function Schottky contact with $\Phi_M=5.4$ eV results in the highest level of hole storage which allows a large electron

tunnelling current and in turn develops more hole storage. Therefore the majority of the V_{AK} bias is dropped across the P-Anode to N-Drift junction forming the high level of voltage $V_{P+ to N-}$. Indeed, the ability of the high work function Schottky to remove any dependence of the P-Anode to N-Drift junction bias from the widely variable N-Drift region resistance is highly desirable. This fact would provide a very stable bias point in terms of V_{AK} at which the P-Anode becomes forward biased as it is unaffected by the state of conductivity modulation within the N-Drift region.

4.4 Effect of using a mixed conductivity type substrate

If the implementation of the JBS minority injector structure is considered within a VDMOSFET, then as shown in figure 4.25 the effect of the channel and P-body can be ascertained through use of a modelled JBS structure in which a mixed conductivity type substrate replicates the effect of the carrier path to ground. In this example case both the doping densities used were equal where $N_a=N_d=1E19\text{ cm}^{-3}$. This is generally not strictly true as the P-body is of a lower acceptor concentration and hence has a higher resistance than the inverted channel for electrons, but the structure gives a first order approximation as to the overall effect. As can be seen through comparison of figure 4.24 with figure 4.25 then the mixed substrate allows the transportation of holes through the substrate.

The resultant I-V characteristics for the JBS diode with a mixed conductivity type substrate is shown in figure 4.26. As can be seen from figure 4.26, the use of a mixed substrate provided a set of I-V characteristics which were very similar to that shown in figure 4.21 a) for the JBS diode without a substrate. This is due to the separated carrier paths in the substrate which prevents any recombination until reaching the cathode Ohmic contact. Thus, the resultant hole storage within the N-Drift region is reduced as shown for the JBS diode model without a substrate in figure 4.20 a). The effect also on the QFN and QFP developed longitudinally within the JBS device is almost identical to the structure without a substrate as can be seen by comparison of figure 4.27 with figure 4.23 a).

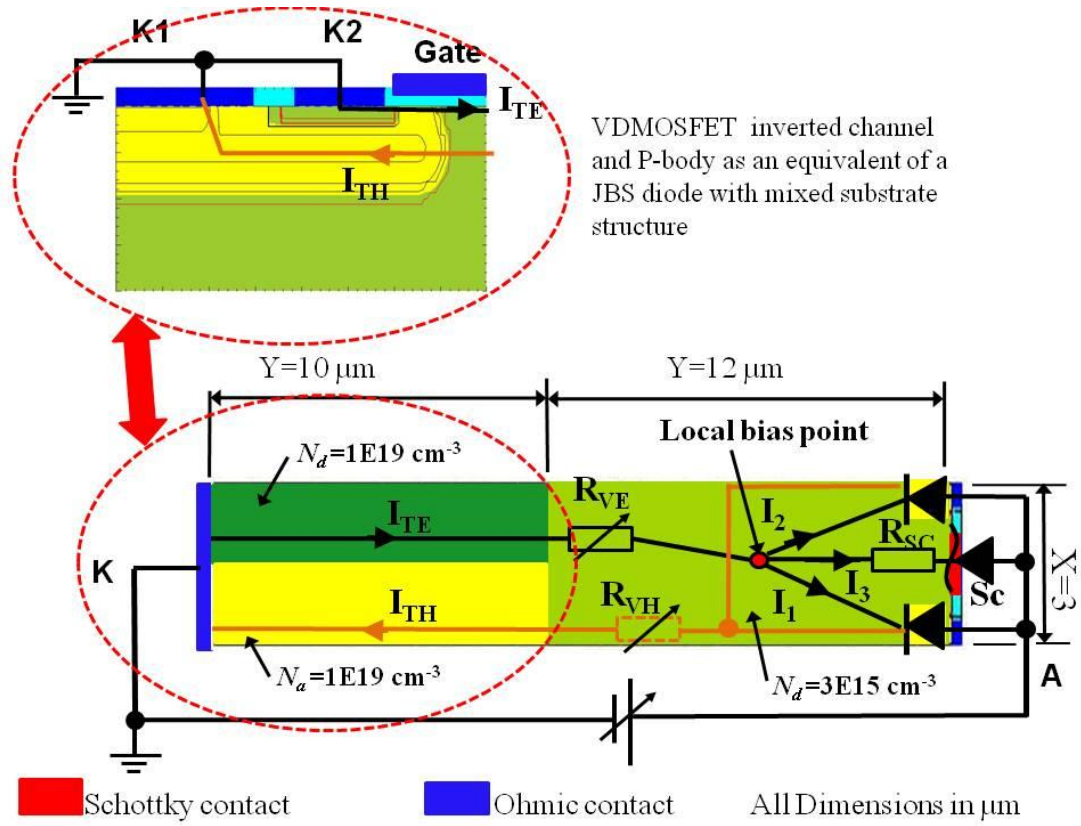


Figure 4.25. Equivalent mixed substrate JBS model of a VDMOSFET implementation.

4.5 Effect of substrate on carrier current flow

Prior to the achieving forward bias of the P-Anode to N-Drift junction, when taking the example of the largest work function Schottky contact ($\Phi_M=5.4$ eV), then the resultant carrier current density can be seen in figure 4.28. This figure provides a direct comparison of the situation at a cut taken at $Y=1.2 \mu\text{m}$ for each of the simulated structures without and with a substrate as shown in figures 4.19 a) and b) as set against that with the mixed substrate shown in figure 4.25. In all cases the bias is set at $V_{AK} = 0.7$ V, which in all cases $V_{AK} < V_i$. Due to the extremely low saturation current of the high work function Schottky contact then in this case the electron current shown in figure 4.28 a) is very low, however this low current led to a fully conductivity modulated N-Drift region, the generated holes in the case of the structures without a substrate and with mixed substrate were allowed to form a small hole current as shown in figure 4.28 b). Whereas, within the donor doped substrate then

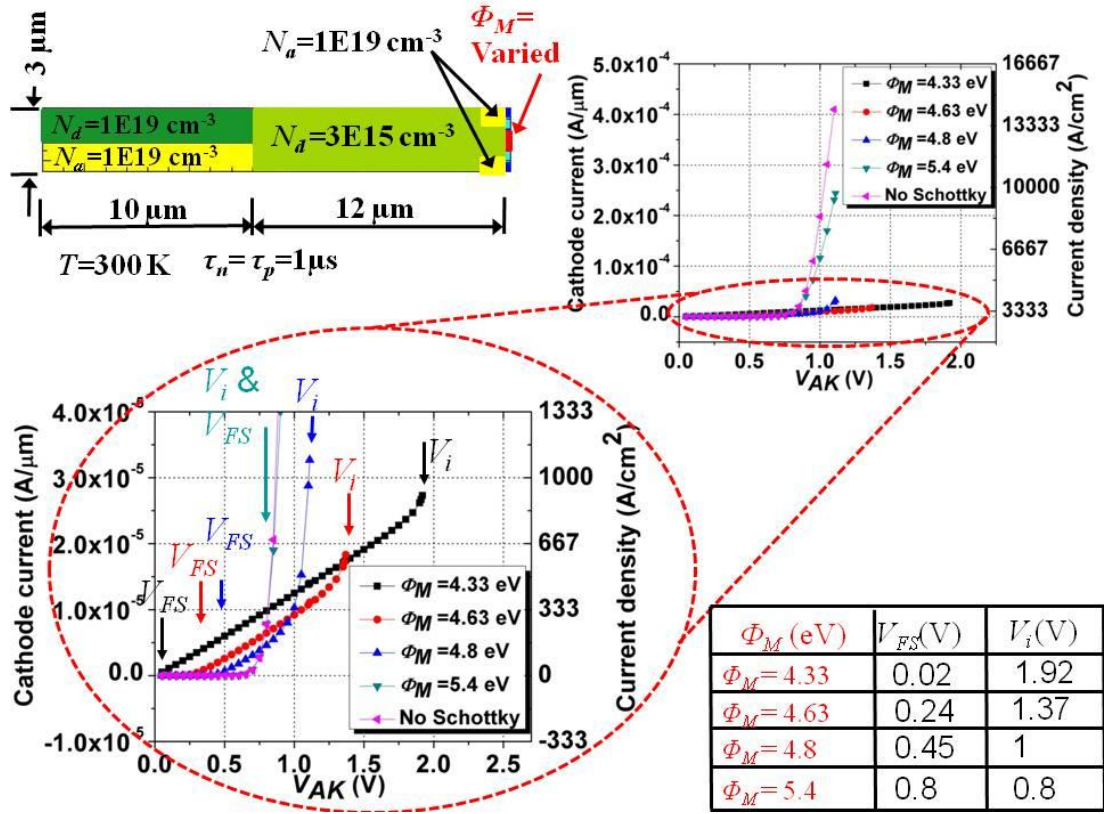


Figure 4.26. Forward I-V characteristics of JBS diodes with a mixed substrate as the Schottky work function (Φ_M) is varied.

effectively a potential barrier to holes was formed which prevented conduction of holes to the cathode. The same comparison, but in the situation when the P-Anode is forward biased ($V_{AK} = 0.9 \text{ V} > V_i$) is shown in figure 4.29. In this case the structure with a degenerately doped donor substrate demonstrates an extremely high electron current in figure 4.29 a) as in this case all the holes recombine in the substrate which forces replacement of the recombined electron via the cathode terminal, hence an increase in the total electron current occurs and the hole current is very low. The JBS diode conduction in this case remained essentially unipolar in nature, but benefited from conductivity modulation.

In the case where there is no substrate, or a mixed conductivity type substrate, then the electron current is 600 A/cm^2 , whereas the hole current is now very high peaking at around 1100 A/cm^2 . This is due to the holes now able to recombine at the cathode Ohmic contact, thus enabling bipolar conduction through the device. The total current (the sum of

the hole and electron current) is hence largest in the bipolar device, thus this device has the lowest on state loss.

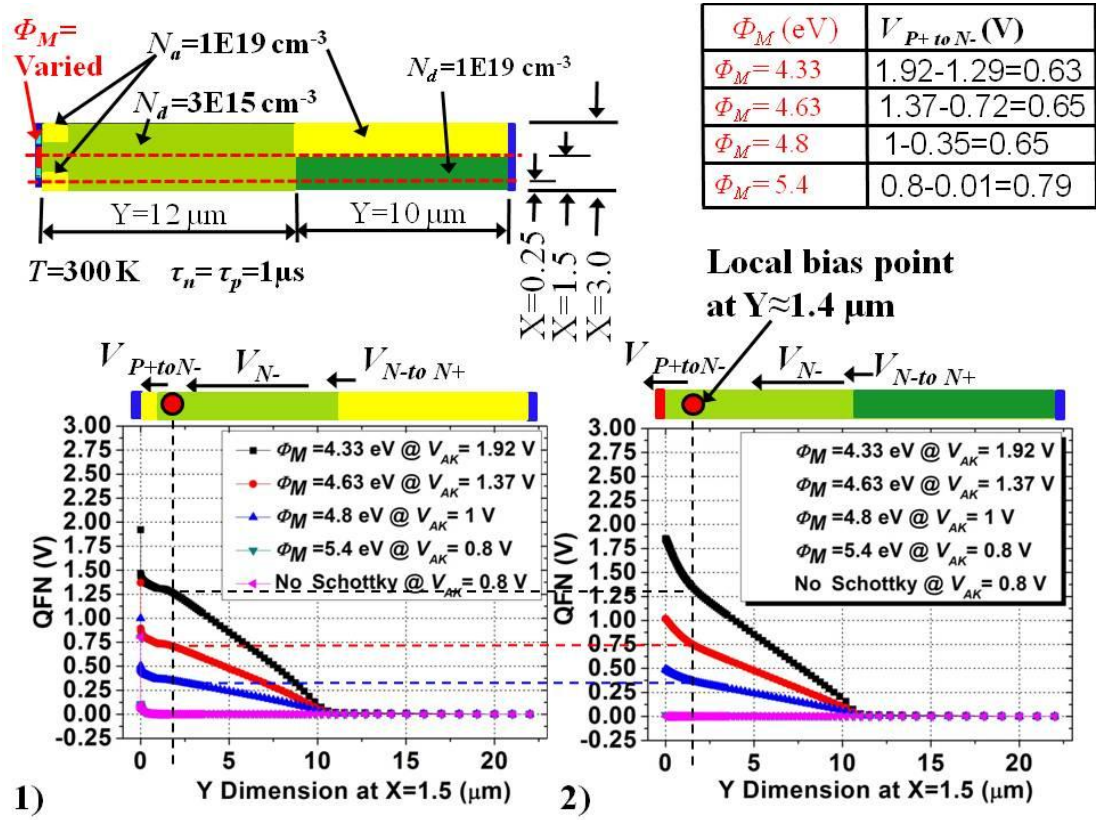


Figure 4.27. Quasi Fermi potential in JBS structure with a mixed substrate as the Schottky work function (Φ_M) is varied.

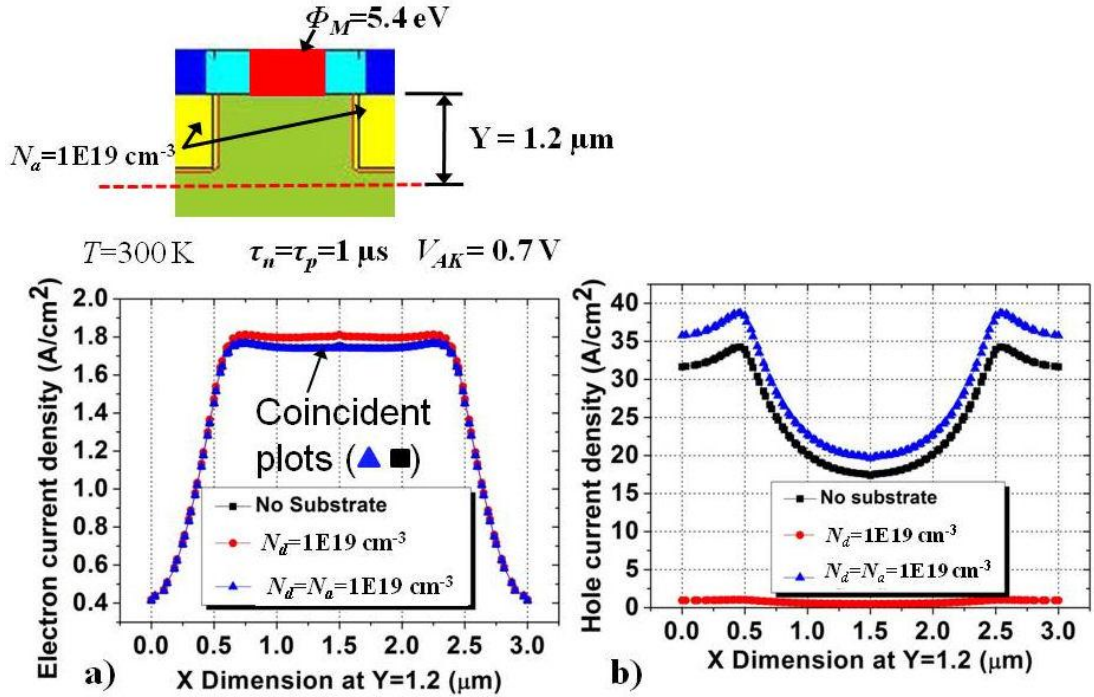


Figure 4.28. Comparison of carrier current prior to forward bias of the P-Anode ($V_{AK} = 0.7 \text{ V}$).

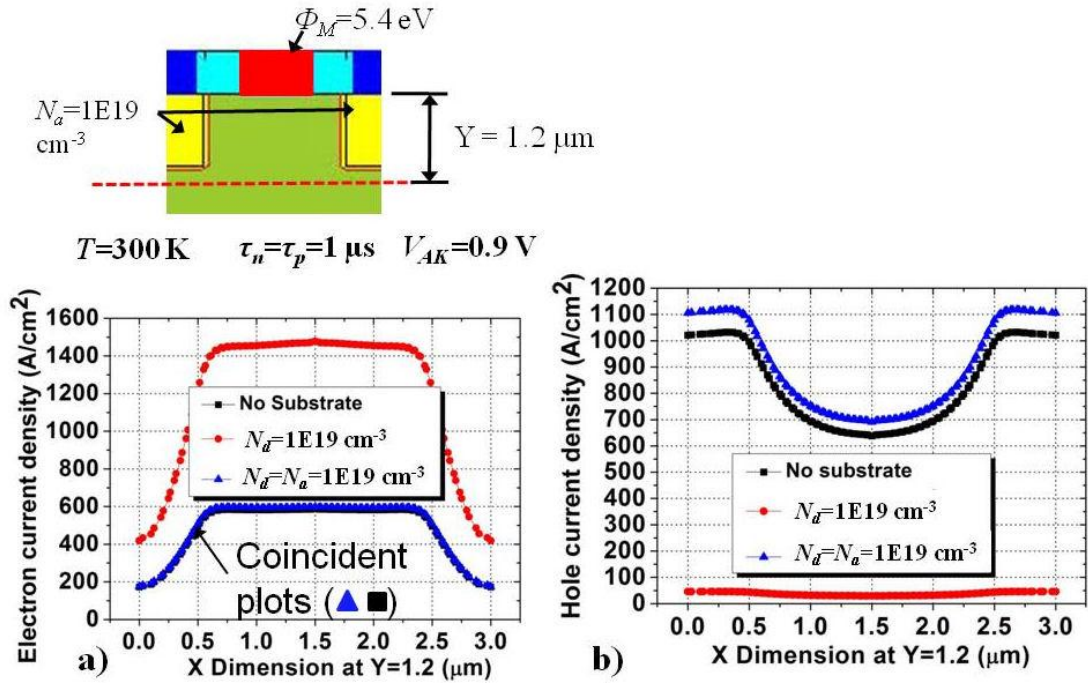


Figure 4.29. Comparison of carrier current following forward bias of the P-Anode ($V_{AK} = 0.9 \text{ V}$).

4.6 Minority carrier injection Summary

It was apparent from both sections 4.2.1, on the P-N junction, and section 4.2.2, on the high work function Schottky diode, that a state of high level injection could be obtained with either of these injection methods into an N-Drift region grown on a substrate which was degenerately doped with donors. Either of these proposed methods could therefore be used to provide a conductivity modulated majority carrier device. However, bipolar conduction could only be achieved within a structure which included a P-Anode (emitter) and one which allowed a flow of holes to the cathode by either removing the donor doped substrate, or by having a substrate of mixed conductivity types. A mixed conductivity type substrate was presented as an equivalent to the use of a P-body and channel of a VDMOSFET to provide a connection to ground. The p type substrate, or P-body, would essentially form a collector of holes to the cathode, whereas the inverted channel would provide a path for electrons from the cathode towards the anode.

Upon review of the JBS diode structure then the use of a merged high barrier height Schottky/P-Anode injector ($\Phi_M = 5.4 \text{ eV}$) on an N-Drift region was proven to provide a

means of repeatable self bias of the P-Anode to N-Drift junction at a local bias point regardless of the level of conductivity modulation occurring within the N-Drift region as a result of stored holes due to the Schottky contact and substrate type. The anticipated structures essentially would provide a PNP BJT function within the core VDMOSFET structure utilising the JBS diode type minority carrier injector as shown in figure 4.30. Such a structure would result in a PNP BJT in either a) a vertical structure or b) a lateral structure. The resultant PNP BJT would enable a high total (bipolar) current flow consisting of both holes and electron transport. The bipolar current flow would provide a further reduction of the specific on state resistance at a given BV level within the VDMOSFET and hence break the 1-D silicon limit as shown in figure 3.27 of Chapter 3.

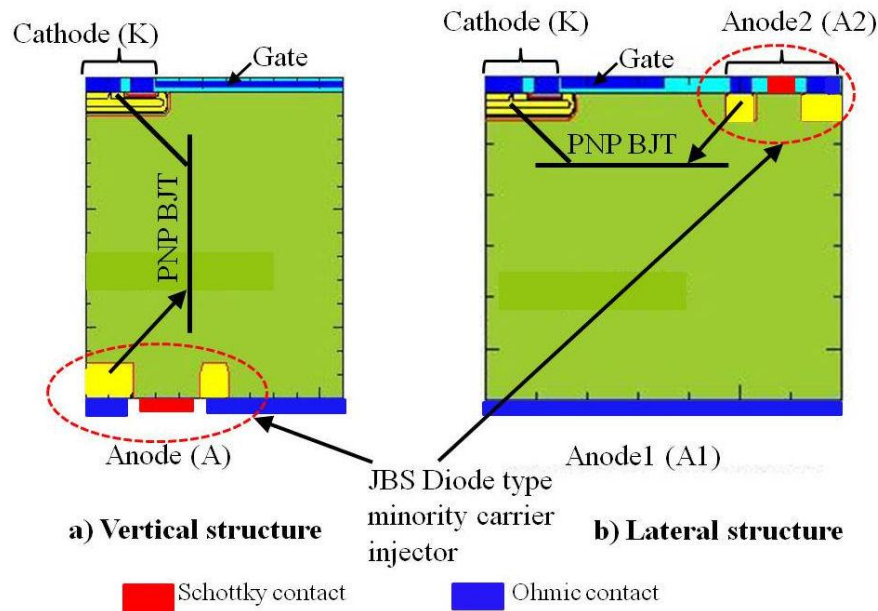


Figure 4.30. Creation of a PNP BJT within a VDMOSFET structure using a JBS diode type minority carrier injector.

The work required to investigate which of the identified minority carrier injected structures (either lateral or vertical) would best meet the aim of the project was as follows:-

- a) Evaluate effect on the potential at the local bias point of the additional path to the positively biased drain for electrons in each of the lateral and vertical cases shown in figure 4.30.

- b) Evaluate the effect of the injector position on Blocking Voltage.
- c) Evaluate best position for the injector so as to provide minimum specific on state resistance $R_{(ON,SP)}$ for the unipolar part of the forward I-V characteristic.
- d) Evaluate the effect of the limited electron source via the MOS channel.
- e) Consider any practical realisation issues and make a considered choice as to which structure and minority carrier injector type would progress into the optimisation stage.
- f) Review the state of the art as regards the achievement of a VDMOSFET which include the benefit of either conductivity modulation or a bipolar conduction capability.

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Chapter 5 | Comparison of injected VDMOSFET structures

5.0 Introduction

Previously within chapter 4, a selection of minority carrier injector structures were reviewed. A merged high barrier height Schottky contact and P-N junction, performing the function of a minority carrier injector, was simulated within a Junction Barrier Schottky (JBS) type diode structure. This structure was shown to not only provide conductivity modulation of the N-Drift region due to the Schottky, but also a large minority carrier (hole) current when a mixed conductivity type substrate was incorporated. Such a mixed conductivity type substrate essentially provided a first order approximation of the equivalent path to ground via a P-body and inverted channel within an N channel enhancement VDMOSFET. Such a structure was demonstrated to provide a higher total current density through the same active area than resulted from the standard unipolar JBS diode structure with the same high barrier Schottky, but fabricated on an N+ substrate. The minority carrier conduction path was via a PNP type bipolar junction transistor (BJT) formed within the VDMOSFET structure. The minority carrier injector or ‘emitter’ of the PNP BJT (as formed by the P-Anode structures) achieved forward bias via a local bias point. The potential of this point was shown to be equivalent to the built in potential (V_{BI}) of the high barrier height Schottky and therefore unaffected by the level of conductivity modulation within the N-Drift region. The P-Anode therefore achieved self biased forward conduction leading to a large minority carrier current flow via the PNP BJT. The point of forward bias of the P-Anode was shown to be reduced (in terms of V_{AK}) by the effect of the increased concentration of stored holes within the N-

Drift region from the conduction of the low saturation current, high barrier height Schottky contact.

This chapter will first review the state of the art bipolar enhanced VDMOSFET devices which offer a bipolar conduction element to ground via the VDMOSFET P-body and inverted channel, such as that often described as an Insulated Gate Bipolar Transistor (IGBT) placed either vertically or laterally. A review as to the effects of a parallel electron path to the $+V_{AK}$ terminal/s, via an Ohmic contact, in addition to that via the Schottky contact, will then be assessed in both the vertical and laterally injected case and an equivalent circuit for each will be provided. The circuit will be used to describe the self bias mechanism used to provide adequate forward bias to the P-Anode injector, or base to emitter junction of the built in PNP BJT. The effect of the injector on the blocking voltage of the hybrid VDMOSFET – IGBT structure will then be reviewed.

5.1 State of the art hybrid VDMOSFET–IGBT structures

In this section a brief review of the state of the art VDMOSFET-IGBT structures will be made where possible via the use of a figure of merit performance chart plotting the specific on state resistance against blocking voltage ($R_{(ON,SP)}/BV$). The state of the art structures reviewed are as follows:-

- a) Reverse Conducting–IGBT, a vertically injected IGBT based hybrid.
- b) The VDMOSFET with lateral injector
- c) The conductivity modulated VDMOSFET
- d) The Schottky injected VDMOSFET
- e) The Minority Carrier Injection controlled Field Effect Transistor (MICFET)
- f) The Injected FLYMOSFET

Each of these structures is shown in figure 5.1.

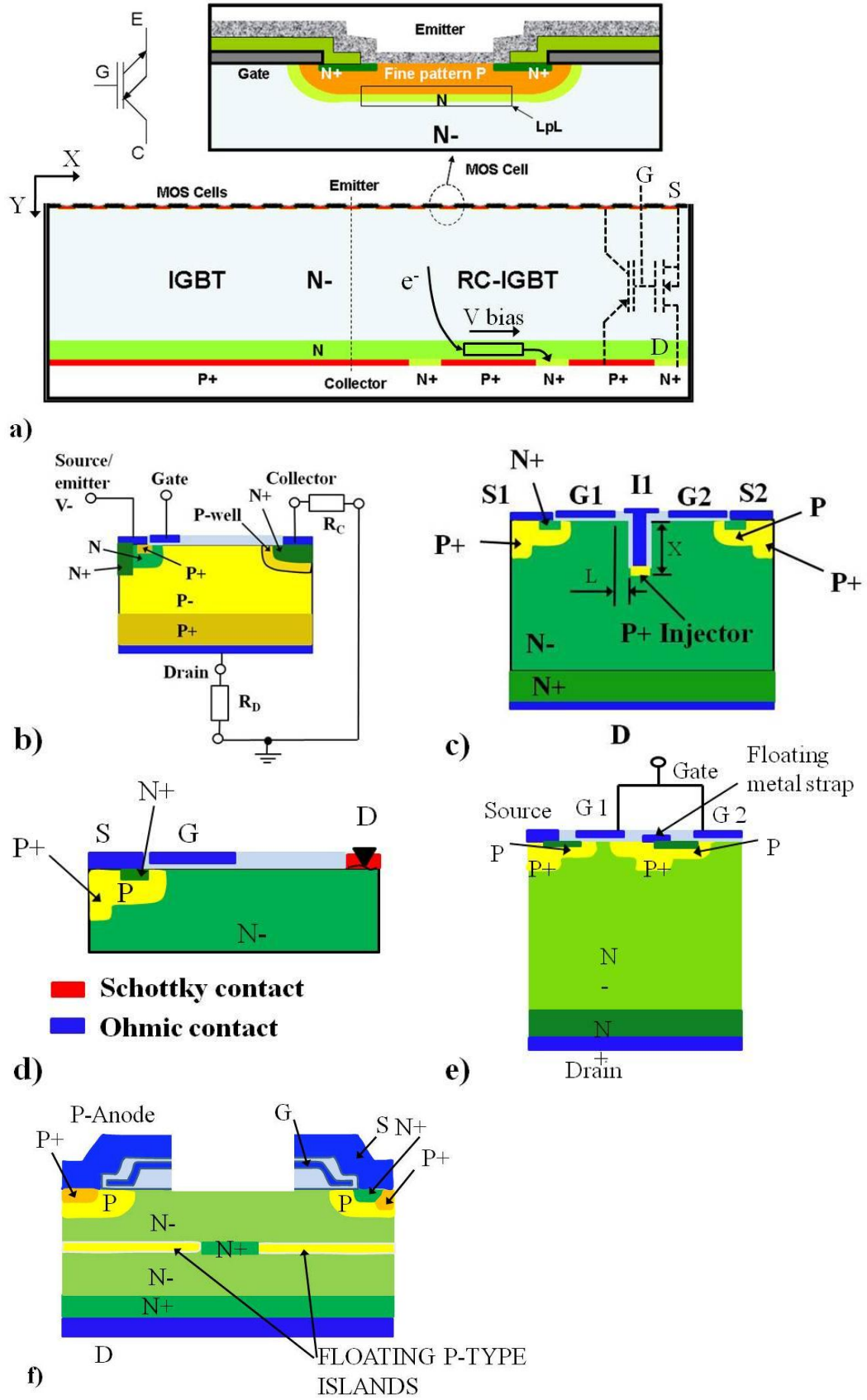


Figure 5.1. a) BIGT concept (Rahimo[1]); b) VDMOSFET with lateral injector (Chow) [2], c) conductivity modulated VDMOSFET (Liu[3, 4]); d) SINFET (Sin[5, 6]); e) MICFET, (Ajit[7, 8]); f) Injected FLYMOSFET (Reynes[9]).

The Reverse Conducting IGBT concept (RC-IGBT) or Bi-mode Insulating Gate Transistor (BIGT) (Rahimo[1]) was created to provide a built in P-N ‘body diode’ into an otherwise standard Non Punch Through (NPT) IGBT structure for use with inductive loads, thus providing an alternative to the use of a separate diode die within an IGBT module. As can be seen in figure 5.1a) the RC-IGBT due to the use of N+ shorts through the P-Anode provides a unipolar VDMOSFET electron path to drain.

The RC-IGBT concept as developed by Rahimo[1] was able to demonstrate the ability to pattern and implant the reverse side of the wafer (collector side). In this case due to the thinned, but still relatively thick drift region ($>150\text{ }\mu\text{m}$), no wafer ‘handle’ was required to support the thinned wafer, thus front to back alignment for patterning was feasible. In addition the feature sizes on the reverse of the wafer were large relative to the front, thus alleviating the need for front to back alignment to fine tolerances. In order to reduce the $R_{(ON,SP)}$ of any VDMOSFET then further wafer thinning would be required to around $60\text{ }\mu\text{m}$ for a 650 V rated device. The current state of the art thinned IGBT supplied by Infineon is $40\text{ }\mu\text{m}$ aimed at the 400 V electric vehicle market, Boving[10]. To supply a hybrid based on the RC-IGBT concept at such a voltage rating would require a ‘handle’ wafer bonded to the top patterned side of thinned wafer during processing, this would prevent front to back alignment of the RC-IGBT device leading to use of grossly aligned large feature reverse structures only, which may limit further optimisation of the N+ short to P+ Anode structures as described by Storasta[11]. An improved optimisation to increase the benefit of the MOSFET within an RC-IGBT type device rated to 1200 V was the subject of the work by Donnellan[12].

On a similar vertical injection theme a United States patent was filed by Francis[13] in 2003, essentially this idea was similar to the RC-IGBT described above, however the design was never realised in practice as it was subjected to the same practical constraints as described for the RC-IGBT regarding front to back alignment of fine geometries coupled with the difficulties surrounding the wafer thickness and resultant drift length issues.

The laterally injected VDMOSFET as shown in figure 5.1 b) was published in 1988 by Chow and Baliga[2]. Laterally adjacent to the normal P-body and channel structure of a VDMOSFET an N+ emitter was diffused into a P-well, the P-well was used to improve punch-through performance. The laterally injected VDMOSFET operated in one of two modes selectable via the resistors R_C and R_D . If R_D was high and $R_C = 0 \Omega$ then the flow of hole current was towards the N + injector (collector of the NPN BJT), the higher the drain resistance the lower the bipolar turn on voltage (V_i). If R_C was high and $R_D = 0 \Omega$ then the flow of holes was via the drain. The larger the value of R_C then the larger the forward voltage drop prior to bipolar start up. These external resistance values dissipated a lot of power and added to the overall $R_{(ON,SP)}$ of the device.

The conductivity modulated MOSFET was investigated by Liu and Plummer[3, 4]. The structure was as per a standard VDMOSFET, but with a P+ injector placed to separate the accumulation region between adjacent p-bodies as shown in figure 5.1 c). The injector depth 'X' was adjusted but only low level injection was achieved.

The Schottky Injected Field Effect Transistor (SINFET) by Sin[5], as shown in figure 5.1 d) was essentially a lateral VDMOSFET, but used a lateral Schottky contact instead of an N+ Drain contact lateral. The forward blocking voltage was reported to be 170V, but due to the Schottky the SINFET device also achieved a reverse breakdown voltage (albeit rather low at 80V) this however, also prevented the SINFET from performing the body diode function as required of any MOSFET controlling inductive loads.

The Minority Carrier Injection Controlled Field Effect Transistor (MICFET) was described by Ajit[7, 8] as shown in figure 5.1 e). Unfortunately, the structure was overcomplicated and, as a result of the large JFET resistance, the $R_{(ON,SP)}$ was high.

Although no technical papers were ever published on the subject, a world patent was filed by Reynes[9] in 2008 to describe a laterally injected version of the FLYMOSFET. This was the laterally injected version of the Floating Island MOSFET (FLYMOSFET or

FLIMOSFET) was a concept first described by Cézac[14] later developed by Roig[15] and then Weber[16]. The patent on the injected version indicates that the device may be rated up to 600 V. The 600 V rating however, would require a large lateral separation dimension between the P-body and the P-Anode which may be preventative to adequate PNP action due to the very wide base width. Although a lateral RESURF type action (first described by Appels[17]), may occur depending on p region thickness leading to a reduction of the lateral distance. The lack of any technical papers following grant of the world patent may indicate that a successful demonstration of the device was not yet completed.

5.1.1 Summary of injected device performance

A summary of the documented device performance in terms of the achieved level of specific on state resistance versus the achieved blocking performance is detailed in figure 5.2. This provides a relative measure which can be used as a figure of merit. Please note that the RC-IGBT could not be plotted on this scale as it was a 3.3 kV rated device. Unfortunately, the forward conduction I-V plot provided by Rahimo[1] was also not sufficiently detailed at low V_{AK} bias to provide an $R_{(ON,SP)}$ figure for the unipolar conduction phase.

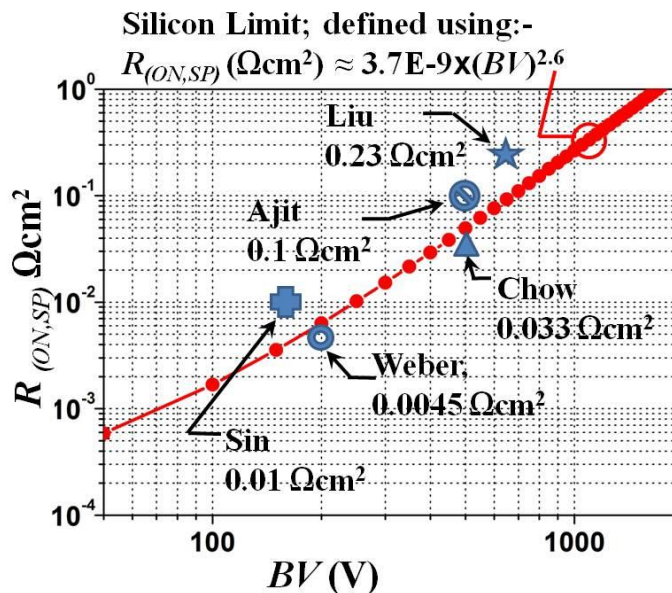


Figure 5.2. Comparison of documented specific on state resistance levels achieved under injected conditions versus achieved blocking voltage.

Clearly from figure 5.2 the SINFET (Sin[5]), the conductivity modulated MOSFET (Liu[4]) and the MICFET Ajit [8] did not achieve bipolar conduction as they all fail to cross the silicon limit line. No performance figures were available for the injected FLYMOSFET type of device from Reynes[9], instead the figures for the FLYMOSFET are provided in unipolar conduction with cross over the silicon limit line by virtue of the reduced drift region resistance. Due to the increased resistive path to drain of the laterally injected version in unipolar mode, then there is no expectation that the injected version will better than the result for the standard FLYMOSFET.

5.2 Proposed hybrid (injected) VDMOSFET structures

As a result of the work described in Chapter 4 then two structures were identified as potential bipolar conduction capable VDMOSFET hybrids as shown in figure 5.3. Both these structures included the Junction Barrier Schottky (JBS) diode type minority carrier injector. The injector includes a high metal work function Schottky barrier contact shown to

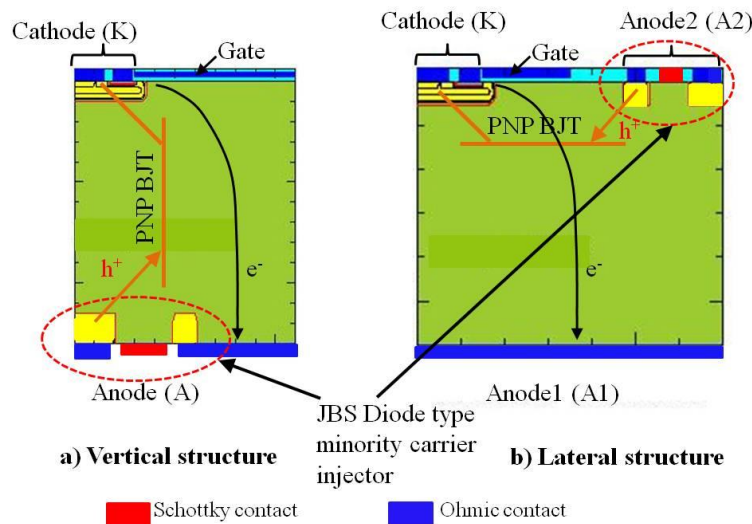
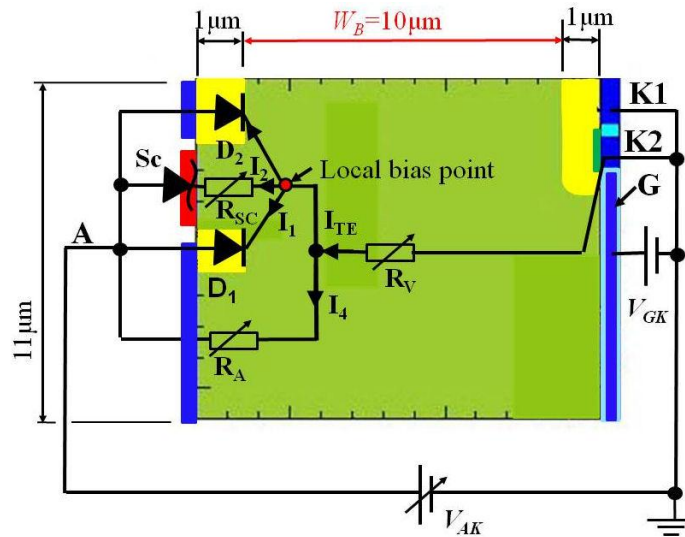


Figure 5.3. Vertical and lateral structures of the bipolar conduction capable VDMOSFET. enable forward biasing of the P-Anode regardless of the state of conductivity modulation within the N-Drift region. Two hypothetical equivalent circuits for each of the lateral and vertical structures of the hybrid will be provided in both unipolar, and bipolar, mode; these will then be verified and used to assess the method of achieving self bias across the emitter –

base junction (V_{EB}) of the two device types. Essentially, the integrated PNP BJT element within the hybrid VDMOSFET structure would be activated as soon as the emitter to base junction achieved sufficient forward bias (V_{EB}). Finally, the importance of the magnitude of V_{EB} achieved will be explained in relation to the PNP performance and the effect of base width.

5.2.1 The equivalent circuit of the vertically injected VDMOSFET

The vertically injected VDMOSFET shown in figure 5.3 includes the PNP BJT conducting holes in parallel with an electron conduction path to the + V_{AK} bias applied to the VDMOSFET drain (or anode of the vertically injected hybrid). The equivalent circuit of this vertical structure of the VDMOSFET in unipolar mode is shown in figure 5.4. As



R_V includes channel, accumulation region, JFET and drift resistances

Figure 5.4. Equivalent circuit within the vertical structure of the injected VDMOSFET hybrid in unipolar mode.

can be seen the voltage developed at the local bias point in relation to the positive voltage applied to the anode (forming V_{EB}) will be dictated by the potential divider set up between the resistance R_V and the voltage developed across the components in parallel (R_A , S_C , D_1 and D_2). R_V also forms the drift region resistance of the vertical PiN diode formed between D_1 (and D_2) via the MOS channel to the N+ cathode. The potential developed across the parallel elements D_1 , D_2 , $S_C + R_{SC}$, and R_A are equal, where R_A is the resistance of the added

electron path to drain (anode). The operation of the Schottky in this structure was to be investigated in relation to the other parallel circuit elements to determine the resultant level of V_{EB} achieved. The equivalent circuit schematic in bipolar mode is shown in figure 5.5 which identifies the PNP BJT integral within the structure.

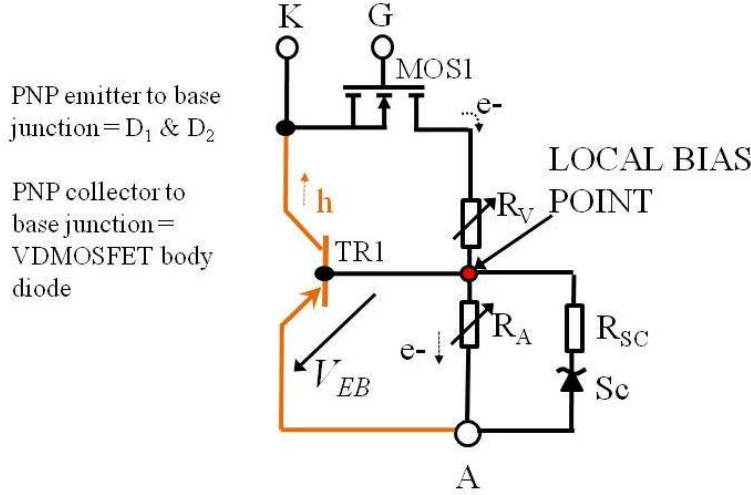


Figure 5.5. Schematic representation of the equivalent circuit in bipolar mode showing the PNP BJT (TR1) and the effect of added Schottky (Sc) on base bias.

5.2.2 The equivalent circuit of the laterally injected VDMOSFET

The equivalent circuit of the laterally injected VDMOSFET in unipolar mode is shown in figure 5.6. Obviously, this differs markedly from that of the vertical structure as there are now two parallel paths to the anode (A1 or A2). However, only the path to anode 2 forms a PiN diode with the resistance R_L forming the N-Drift resistance. The equivalent circuit in a) unipolar mode and b) bipolar mode for the laterally injected VDMOSFET is shown in figure 5.7 again, showing the integral PNP BJT, but on this occasion although the half cell dimensions are identical, the base width (W_B) of the PNP BJT in the lateral structure is much reduced from $W_B = 10 \mu\text{m}$ in the vertical structure, to $W_B = 3 \mu\text{m}$. The importance of the base width (W_B) will be discussed later. Again, the operation of the Schottky in this lateral structure is critical and was investigated in relation to the other circuit elements to determine the resultant level of V_{EB} achieved.

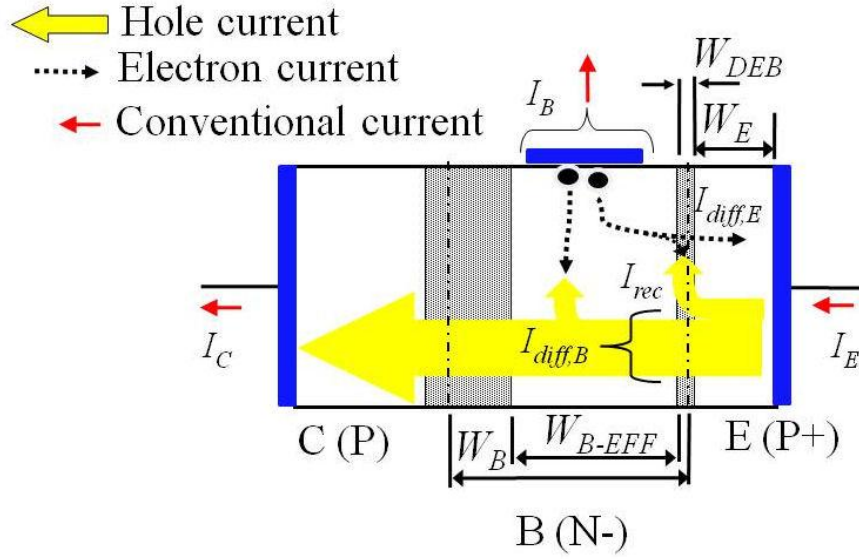


Figure 5.8. Representation of the PNP BJT contained within the hybrid structure.

A PNP BJT is shown in figure 5.8, together with the associated carrier currents and terminal currents. The measure of PNP BJT performance within the hybrid is the common base gain (α or h_{FB}), which itself is dependent upon the emitter injection efficiency (γ) and base transport factor (α_T). The theory of gain within a PNP BJT was described by Grove[18]. According to Grove the common base gain (α or h_{FB}) is given by equation 5.1.

$$\alpha \equiv h_{FB} \equiv \frac{I_C}{I_E} = \gamma \alpha_T \quad (5.1)$$

Where I_C is the collector current, I_E is the emitter current (total emitter current). The base transport factor, α_T , describes the relationship between the injected hole current and the amount of hole current actually collected after traversing the base region of width, W_B , with a minority carrier diffusion length in the base region (L_{pB}) prior to recombination as shown in equation 5.2.

$$\alpha_T = \frac{1}{\left(\cosh \frac{W_B}{L_{pB}} \right)} \quad (5.2)$$

The emitter injection efficiency (γ) according to Grove[18] is the relationship between the injected hole diffusion current into the base and the electron current into the emitter (I_E) as shown in equation 5.3.

$$\gamma = \frac{I_{diff,B}}{I_E} \quad (5.3)$$

Where $I_{diff,B}$ is the diffusion current of holes in to the base from the emitter:-

$$I_{diff,B} = qD_{pB} \frac{n_i^2}{N_{dB}W_B} e^{\left(\frac{qV_{EB}}{kT}\right)} A \quad (A) \quad (5.4)$$

(N_{dB} is the donor concentration in the PNP base region, D_{pB} is the diffusivity of holes in the base). And I_E is the emitter terminal current given by:-

$$I_E = I_{diff,B} + I_{diff,E} + I_{rec} \quad (A) \quad (5.5)$$

The electron current into the emitter ($I_{diff,E}$) is given by:-

$$I_{diff,E} = qD_{nE} \frac{n_i^2}{N_{aE}W_E} e^{\left(\frac{qV_{EB}}{kT}\right)} A \quad (A) \quad (5.6)$$

(N_{aE} is the acceptor concentration in the PNP base region; D_{nE} is the diffusivity of electrons in the emitter). The recombination current (I_{rec}) in the depletion region (of width W_{DEB}) of the emitter to base junction (of area A) is given by:-

$$I_{rec} = 0.5q \frac{n_i}{\tau_{Sc}} W_{DEB} e^{\left(\frac{qV_{EB}}{2kT}\right)} A \quad (A) \quad (5.7)$$

Where τ_{Sc} is the carrier lifetime in the emitter to base depletion region.

As can be seen from equations 5.1 and 5.3 to 5.7 all feature an exponential function of V_{EB} , therefore the higher the V_{EB} then the higher the injection efficiency. In addition equation 5.2 highlights the reason why base width (W_B) is important to a PNP BJT. Essentially the base width (W_B) needs to be as small as possible to ensure that a high percentage of minority carriers are collected after traversing the base.

5.3 Achieving self bias of the vertically placed injector

This section will show the I-V characteristics obtained from a range of different vertically injected structures. The various structures will be used to demonstrate the effect of P-Anode length and the function of the Schottky in achieving sufficient forward bias (V_{EB}) across the emitter to base junction. The use of plots of the quasi Fermi potential of electrons (QFN) developed within the structures will show the position of the local bias point and the resultant emitter to base bias developed (V_{EB}).

Two vertical structures of varying P-Anode length were used as the basis of the investigation these lengths were: - 3.5 μm and 6 μm . For each P-Anode length a number of different structures were trialled to assess the role of the Schottky contact. For the 3.5 μm P-Anode length the various structures were as follows:-

- 1) Merged Schottky contact ($\Phi_M=5.4$ eV)
- 2) Merged Ohmic contact ($\Phi_M=4.1$ eV)
- 3) Solid P-Anode

For the P-Anode length of 6 μm two structures were assessed as follows:-

- 1) Merged Schottky contact of varying metal work function (Φ_M)
- 2) Solid P-Anode

Each of the above structures was compared against the original optimised VDMOSFET resulting from chapter 3. The I-V characteristics relating to the P-Anode structures of length 3.5 μm are shown in figure 5.9. The I-V characteristics relating to the two 6 μm P-Anode structures are shown in figure 5.10.

On comparison of figure 5.9 with 5.10 then the difference in the bipolar start up voltage (V_i) is due to the length of the P-Anode as a result of the resistive bias method as shown in figure 5.11 for the merged Schottky injectors (of both 3.5 μm length and 6 μm length). From figure 5.9 then the electron current required to forward bias the 3.5 μm P-Anode is around 590 A/cm², which occurs at $V_{AK} = V_i = 2.75$ V, whereas for the 6 μm the current at $V_{AK} = V_i = 1.75$ V was only 364 A/cm² due to the extra length. The potential

developed in a semiconductor due to drift current is described by Parker[19] and Pierret[20]. The voltage developed across the half cell as shown in figures 5.11 a) and b) requires to be multiplied by 2 to obtain the potential across the full cell (the full injector length therefore is 7 and 12 μm respectively).

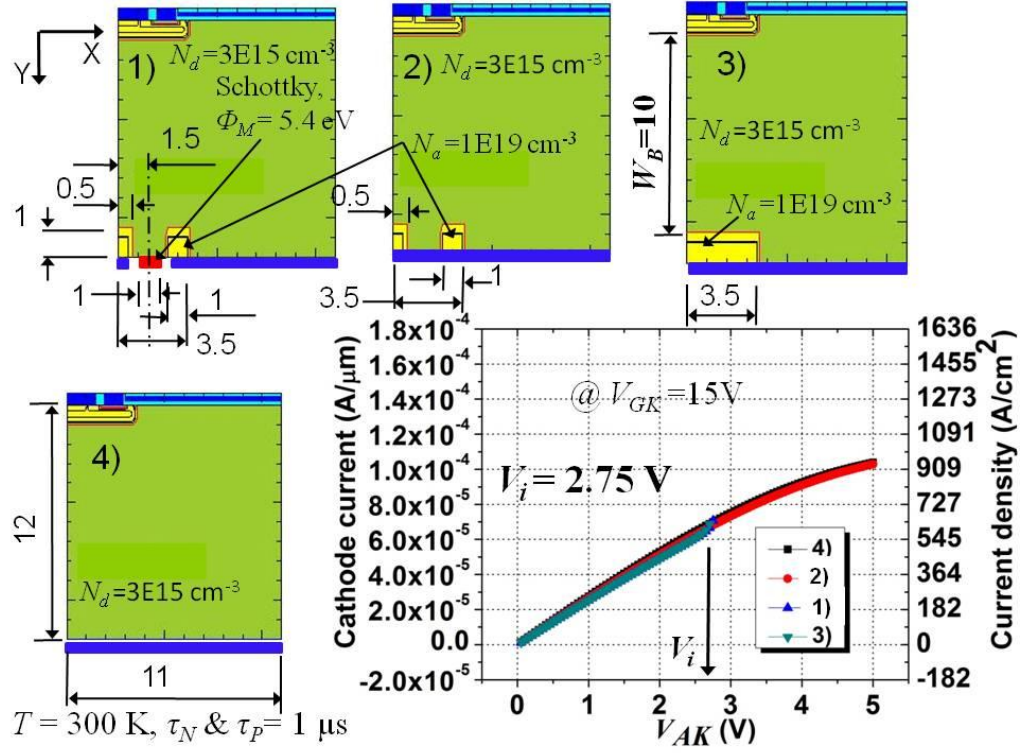


Figure 5.9. Resultant I-V characteristics of an injected MOSFET using a 3.5 μm long injector.

Clearly from the QFN results as shown in figures 5.11 a) and b) the resultant potential developed across the P+ to N- junction ($V_{P+ \text{ to } N-} = V_{EB}$) increases with terminal voltage (V_{AK}). The QFN plots also identify the effect of current density which increases with V_{AK} as each increment in V_{AK} provides an increase in QFN as seen through comparison with the relevant I-V characteristic in figures 5.9 or 5.10. As regards the development of the lateral bias across the P+ to N- junction then clearly the effect of inserting a high barrier height Schottky into the P-Anode to form a merged injector of the same length is minimal as shown in figure 5.12.

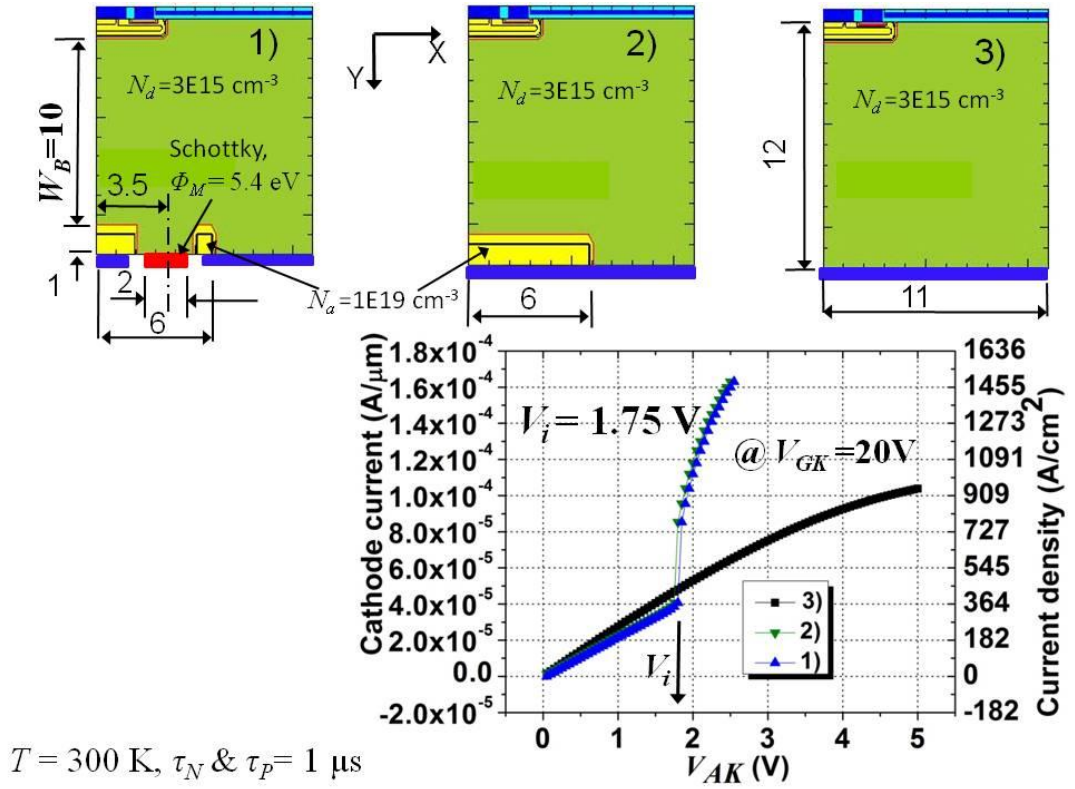


Figure 5.10. Resultant I-V characteristics of an injected MOSFET using a 6 μm long injector.

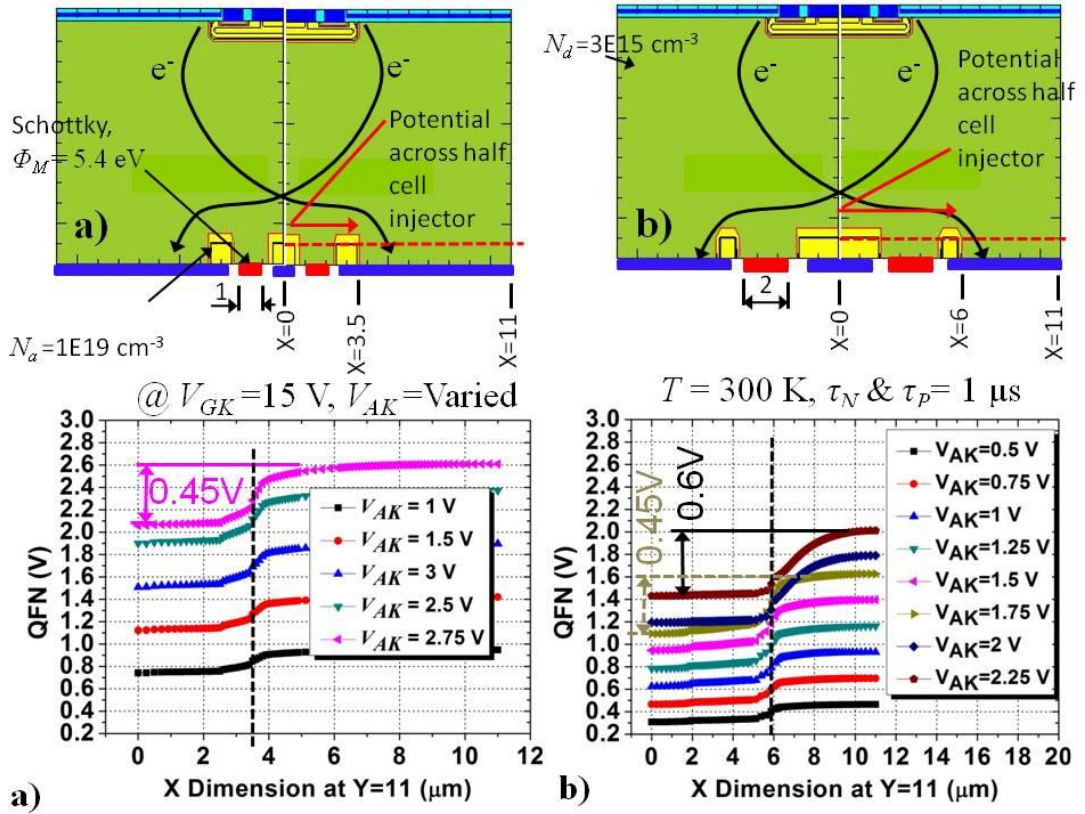


Figure 5.11. QFN plot showing V_{EB} bias developing across a) 3.5 μm and b) 6 μm long merged Schottky P-Anode with increasing V_{AK} .

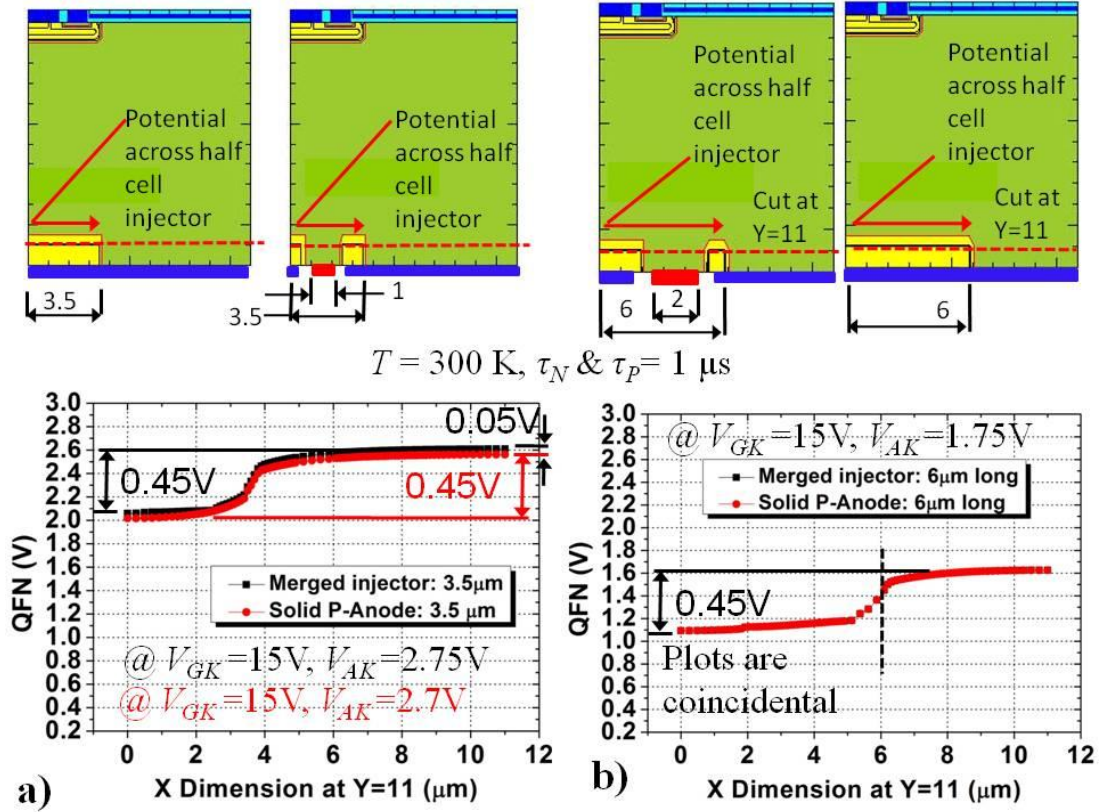


Figure 5.12. QFN plot showing V_{EB} bias developing across a) 3.5 μm , $V_{AK}=2.75 \text{ V}$ and b) 6 μm , $V_{AK}=1.75 \text{ V}$ long merged Schottky P-Anode.

The lateral voltage developed across the vertically placed P-Anode continues to rise with current density as indicated in figure 5.11 b) as the injector voltage rises from 0.45 V at the start up of bipolar conduction (V_i) to 0.6 V at $V_{AK}=2.25 \text{ V}$. This obviously ensures that the bias developed across the base to emitter junction (V_{EB}) increases despite conductivity modulation within the base region. However, the longitudinal voltage across the injector as dictated by the local bias point cannot reach 1.2 V as it is limited by the peak level of carrier concentration achieved within the PNP BJT base region as defined in equation 5.8, where

$p_n = n_n$ when conductivity modulated, and $n_n = N_d$ in unipolar mode (N_d in this case = $3\text{E}15 \text{ cm}^{-3}$).

$$V_{p+toN-} = V_{EB} = \frac{kT}{q} \ln \left[\frac{p_n n_n}{n_i^2} \right] \quad (5.8)$$

From unipolar mode, as described by Baliga[21], eventually due to low level injection from the P-Anode as a function of developed $V_{P+ to N-} = V_{EB}$) then p_n becomes significant relative to N_d . When $p_n = N_d$ then the P-Anode is biased on at a calculated voltage of $V_{EB}=0.8$ V and a high level injection state is achieved, thereafter the electron concentration (n_n) = p_n , and the base region of the PNP BJT becomes conductivity modulated. The hole concentration in the base region as compared to the resultant longitudinal plot of QFN at $X=3$ μm , indicating the local bias point position and hence the level of base to emitter bias (V_{EB}) achieved, are shown in figure 5.13.

As can be seen in figure 5.14 showing the longitudinal quasi Fermi potential for electrons (QFN) at $V_{AK}=1.75$ V and figure 5.15 at $V_{AK}=2.25$ V for the 6 μm long merged Schottky and solid P-Anode injector the effect of the high barrier height Schottky is to maintain the bias (V_{EB}) at 0.85 V which is identical to that of the solid P-Anode. As can be seen the local bias position adjusts to coincide with the volt drop across the parallel elements D_1 , D_2 , S_C & R_{SC} and R_A from the equivalent circuit shown in figure 5.9.

In the comparison of the Schottky width in figure 5.12 a) to 5.12 b) then the width of the Schottky was also seen to have no effect with a high metal work function Schottky ($\Phi_M = 5.4$ eV). The effect of changing the work function (Φ_M) and hence barrier height (Φ_B), now required investigation.

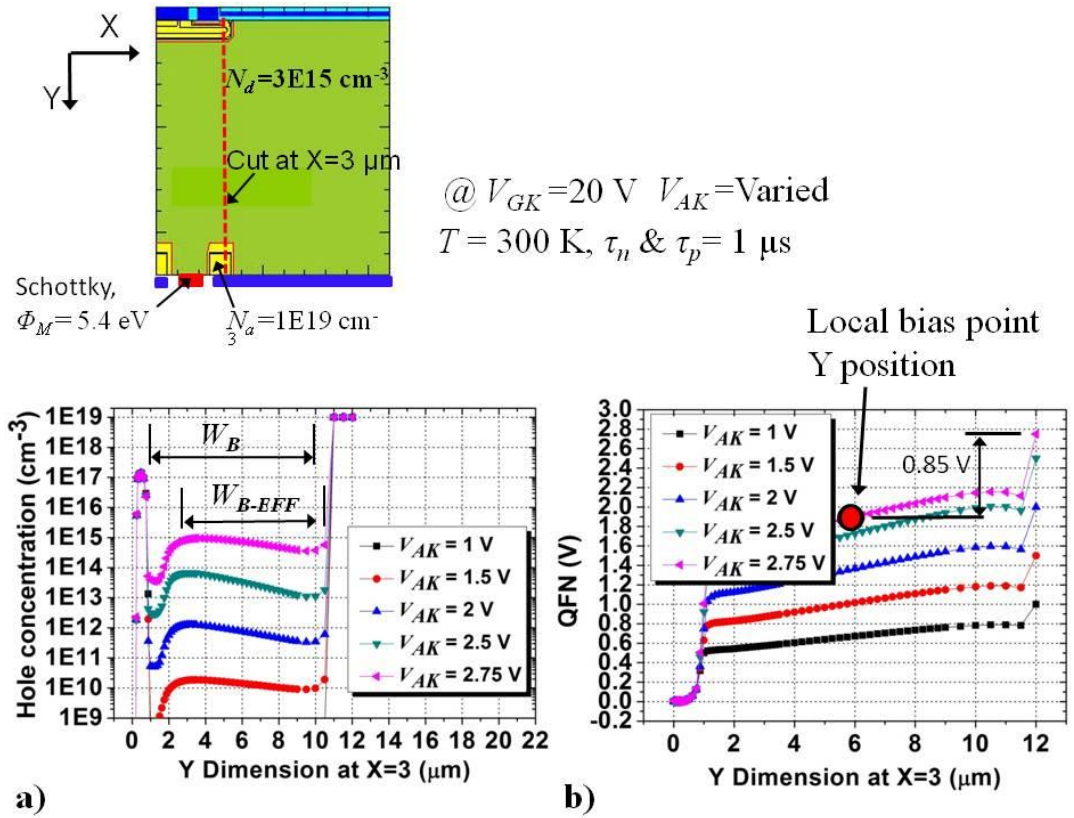


Figure 5.13. a) PiN diode minority carrier injection and b) corresponding P+ to N- junction potential.

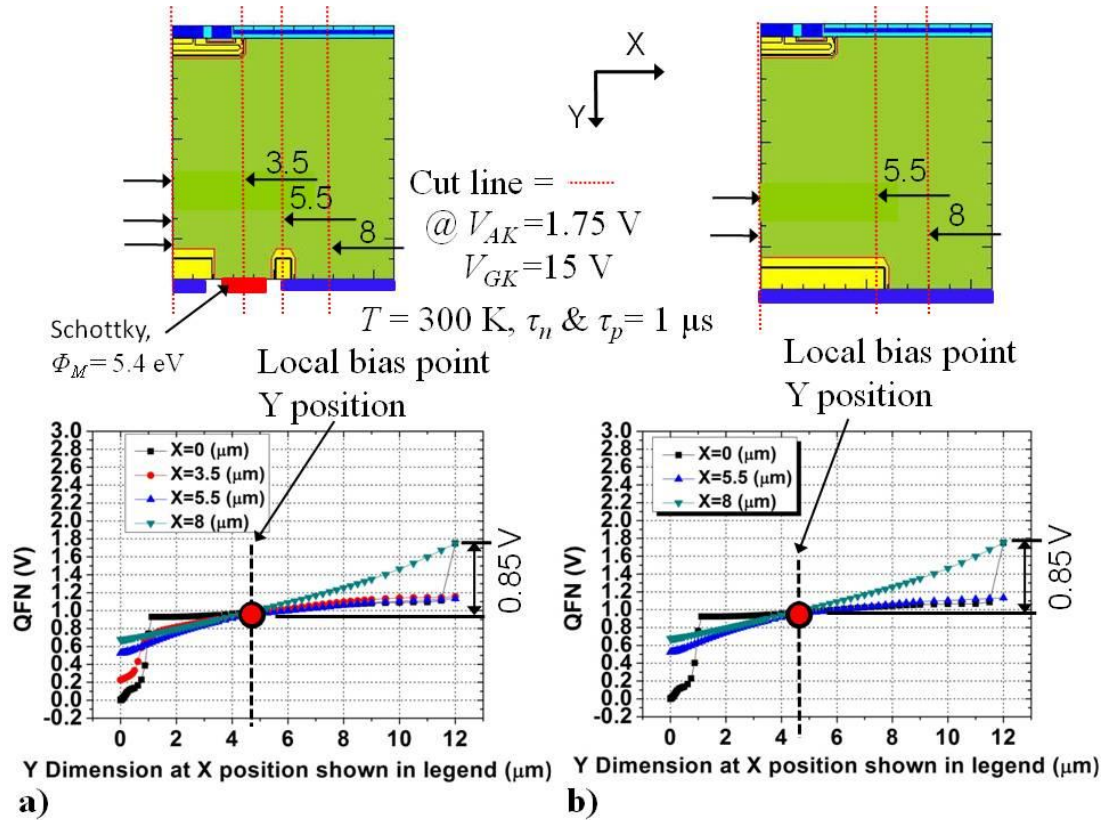


Figure 5.14. QFN plots comparing local bias point voltage between 6 μm long a) merged Schottky injector and b) solid injector at $V_{AK} = 1.75 \text{ V}$.

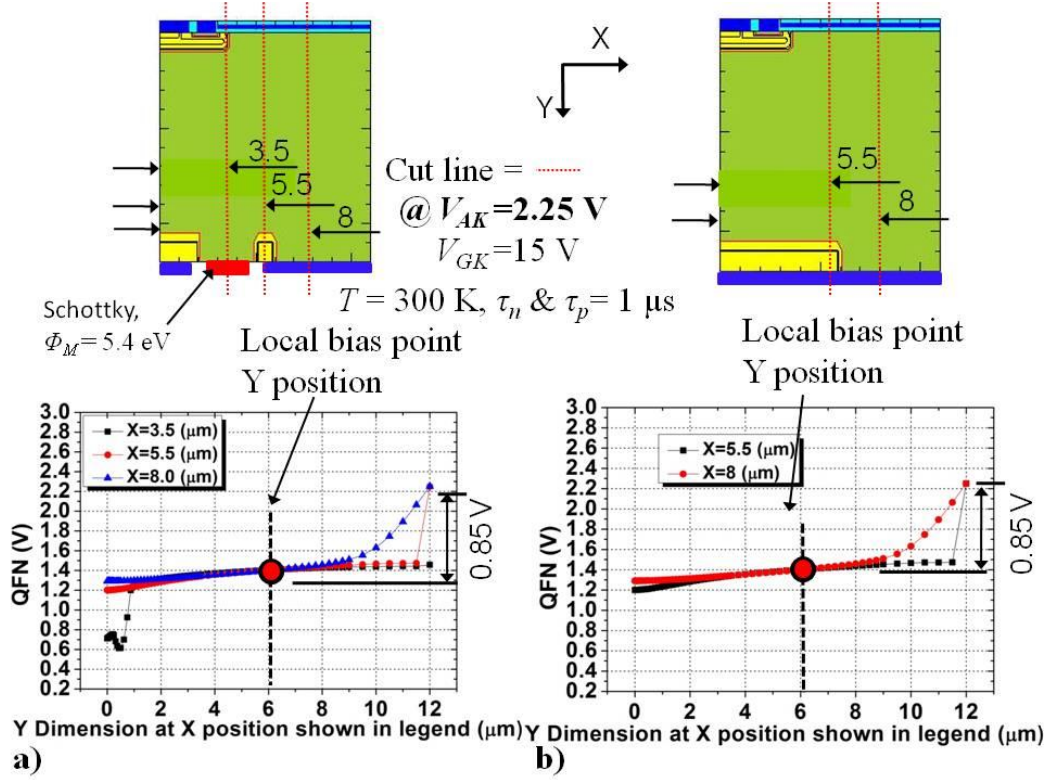


Figure 5.15. QFN plots comparing local bias point voltage between 6 μm long a) merged Schottky injector and b) solid injector at $V_{AK}=2.25\text{ V}$.

5.4 Effect of metal work function in the vertically placed injector

The effect of the metal work function of the Schottky contact within the vertical structure of the hybrid can be seen in figure 5.16 which shows the resultant I-V characteristics as the metal work function (Φ_M) is altered. The contact was varied in the range Ohmic contact ($\Phi_M=4.1\text{ eV}$) to $\Phi_M=5.4\text{ eV}$ (PtSi). The comparison between the resultant current via the figure 5.17 b), for the $\Phi_M=4.8\text{ eV}$, demonstrates the reason why the bipolar start up voltage (V_i) increases with decreased Φ_M . Effectively the lower the work function the lower the V_{AK} bias at which conduction begins via the Schottky contact, as indicated by position (1) in each Schottky contact shown in figure 5.17 a) for the $\Phi_M=4.6\text{ eV}$, and plot. The conducting Schottky contact serves to divert some of the biasing electrons, thus higher current density is required to bias on the shortened effective length of the P-Anode. The electron diversion also prevented P-Anode1 from becoming forward biased in figure 5.17 a) as more of the current is diverted via the conduction of the lower barrier height Schottky. P-Anode 2

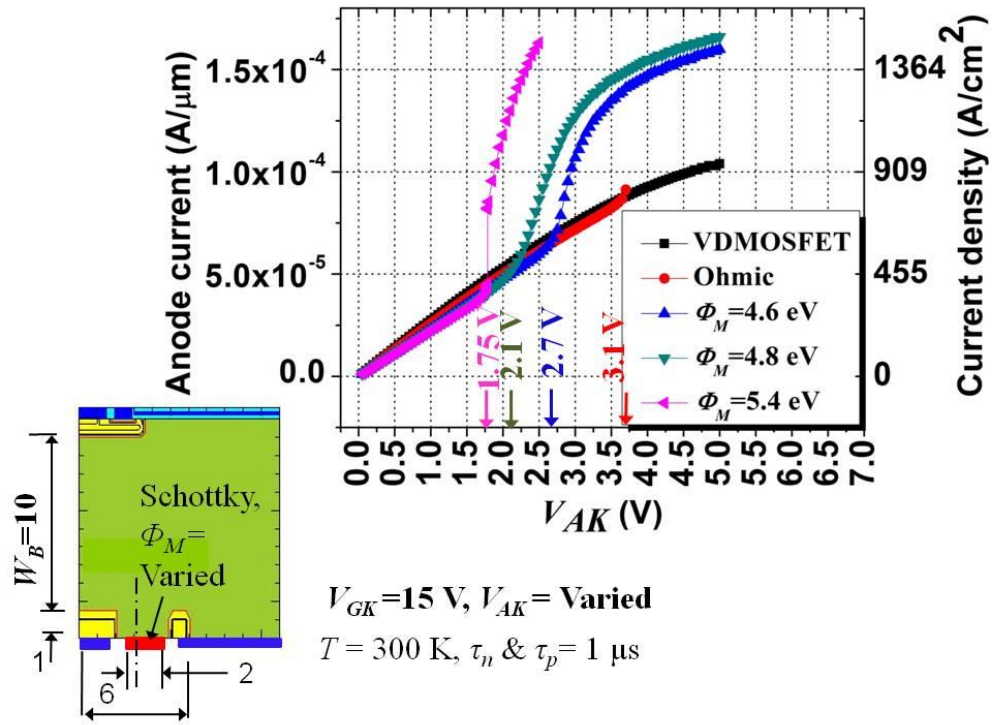


Figure 5.16. Effect of varying the metal work function on vertical hybrid I-V characteristics.

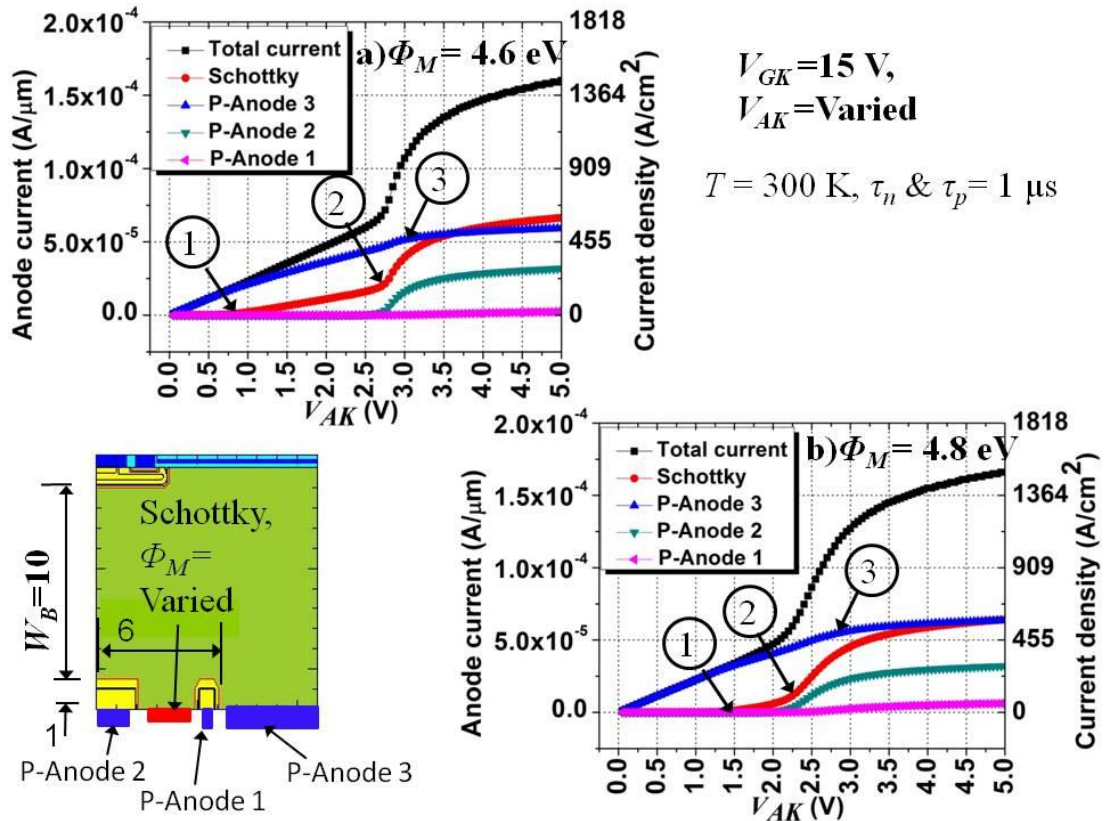


Figure 5.17. Comparison of anode current using Schottky with Φ_M = a) 4.6 eV, b) 4.8 eV.

becomes forward biased at the V_{AK} level indicated at position (2), this occurs in the manner as described by Rhoderick[22] wherein the Schottky depletion minimises due to the conductivity modulation allowing an increased current flow over the barrier, as described in chapter 4. This puts an added drain on the electron supply and yet the MOS channel is limited by the geometry of the channel and the level of inversion. The limitation in the supply of electrons at $V_{GK}=15$ V begins at the V_{AK} level indicated at position (3). Thereafter the hybrid device saturates as the carrier concentration levels are now fixed. From figure 5.16 it is clear that the highest barrier height allows the lowest bipolar start up voltage (V_i) in terms of V_{AK} and offers the lowest Schottky current drain allowing increased electron current to the PNP-BJT emitter ($I_{diff,E}$) and proportionally larger hole current ($I_{diff,B}$). The resultant three dimensional plots of hole concentration at various levels of V_{AK} (with $V_{GK}=15$ V) within the vertical structure of the merged Schottky injected hybrid with $\Phi_M=5.4$ eV and 6 μ m long injector is shown in figure 5.18.

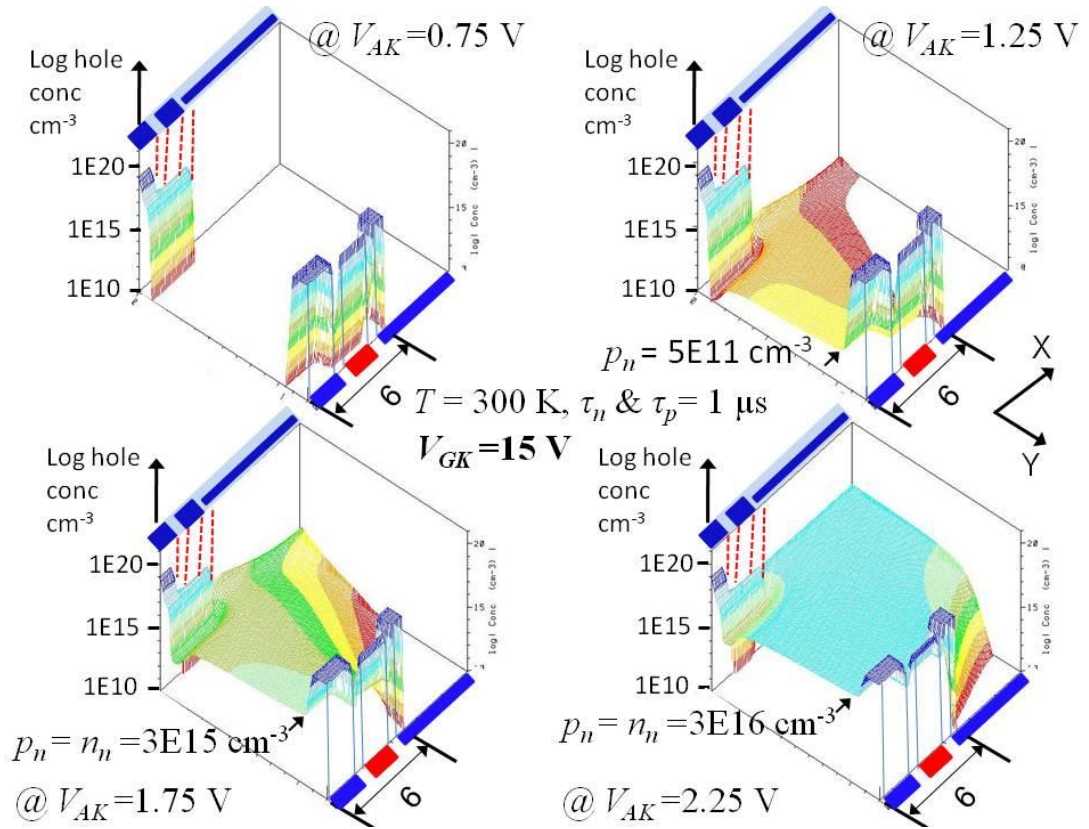


Figure 5.18. Resultant hole concentration within the vertical structure of the injected hybrid with a 6 μ m long injector ($\Phi_M=5.4$ eV) at various increments of V_{AK} bias.

5.5 Achieving self bias of the laterally placed injector

In this section the intention is to describe how the P-Anode injector becomes forward biased within the lateral hybrid structure enabling transition from unipolar to bipolar mode.

If consideration is given to the lateral electron path from the N+ cathode to the degenerately doped P-Anode via the inverted channel then the structure and equivalent circuit is shown in figure 5.19. As described in section 5.4 if the MOS channel is inverted then the analogy of a lateral PiN diode can be used. At $V_{AK}=0.5$ V the PiN structure is in the low level injection mode, figure 5.19 a) shows the progressive increase with bias of the hole concentration from $P_{no} \approx 1E4 \text{ cm}^{-3}$ at equilibrium (with $N_d=3E15 \text{ cm}^{-3}$). The resultant volt drop across the P-Anode to N-Drift region junction ($V_{P+ \text{ to } N-}$) follows the relationship detailed in equation 5.8 as dictated by the relative carrier concentrations. The high injection regime is entered when $V_{EB} = V_{BI}$ of the P-Anode to N-Drift region junction. The plot of potential in figure 5.19 b) shows the potential difference across the P+ to N- junction spaced charged region, transition into the high injection regime occurs when the reduced potential difference, indicated when $V_{P+ \text{ to } N-} = V_{EB}$, approached V_{BI} of the junction. This relationship is described in equation 5.9, as affected by the volt drop across the PiN drift region V_{N-} , of

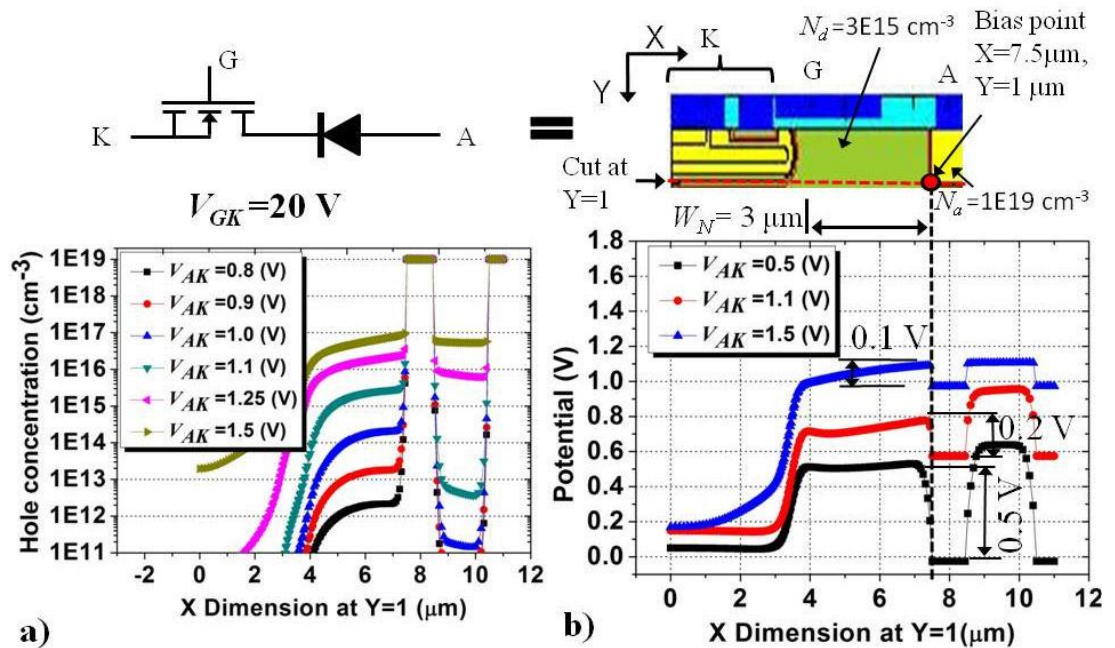


Figure 5.19. Forward biasing of lateral PiN diode structure a) resultant hole concentration, b) resultant potential at local bias point.

width W_N , where $W_N = W_B$, and the applied terminal bias (V_{AK}).

$$V_{BI} - V_{P+toN-} = V_{BI} - (V_{AK} - V_{N-}) \quad (5.9)$$

Where V_{N-} is the resistive volt drop across the drift length, (W_N). A means of calculating V_{N-} is shown in equation 5.10.

$$V_{N-} = R \times I = \rho \frac{W_N}{A} \times J_{TN} \quad (V) \quad (5.10)$$

Where $W_N = 3E-4$ cm of drift region, A in this case is area of P-Anode ($1E-8$ cm²). J_{TN} is the current density within the N-Drift region during the low injection regime, which was derived by Baliga[21] to be calculated as shown in equation 5.11.

$$J_{TN} = \frac{qD_p p_{no}}{L_{pB}} \left(e^{\left(\frac{qV_{EB}}{kT} \right)} - 1 \right) \quad (A/cm^2) \quad (5.11)$$

For example if ($V_{N-} = V_{AK} = 0.5$ V) then the full V_{BI} has yet to be overcome by further increase in V_{AK} . V_{AK} in this case would need to be increased to 1.3 V to allow $V_{P+toN-} = V_{EB}$ to overcome the built in potential of the junction (if V_{N-} remained constant).

In respect to the equivalent circuit for the unipolar mode, as shown in figure 5.7 a), then the PiN diode of figure 5.19 encapsulates the elements R_L and D_1 . Similarly, the same applies in the Kirchhoff equivalent circuit shown in figure 5.20. The verification of the equivalent circuit at an applied bias $V_{AK} = 1.1$ V is shown in terms of the resultant quasi Fermi potential for electron plots shown in figure 5.21. The intersection of the cut lines at $X=4$ and $Y=0.05$ μm of figure 5.22 forms ‘Node1’ as indicated within the Kirchhoff equivalent circuit of figure 5.20. The resultant band diagrams for the unipolar electron current flow path are shown in figure 5.22, these depict how the built in potential of the P+ to N- junction of the PiN diode (D_1) is overcome through carrier concentration change on the N- side of the junction.

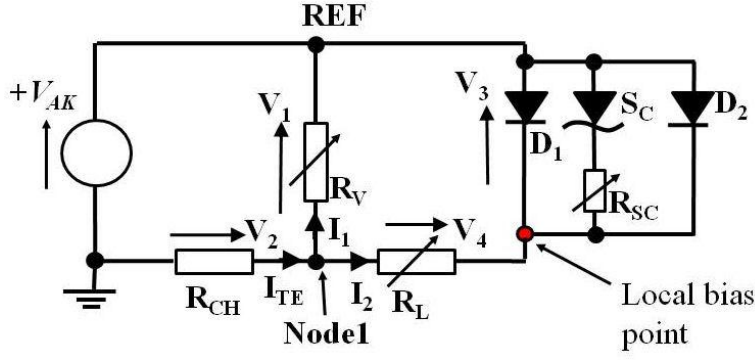


Figure 5.20. Kirchhoff equivalent circuit of laterally injected hybrid.

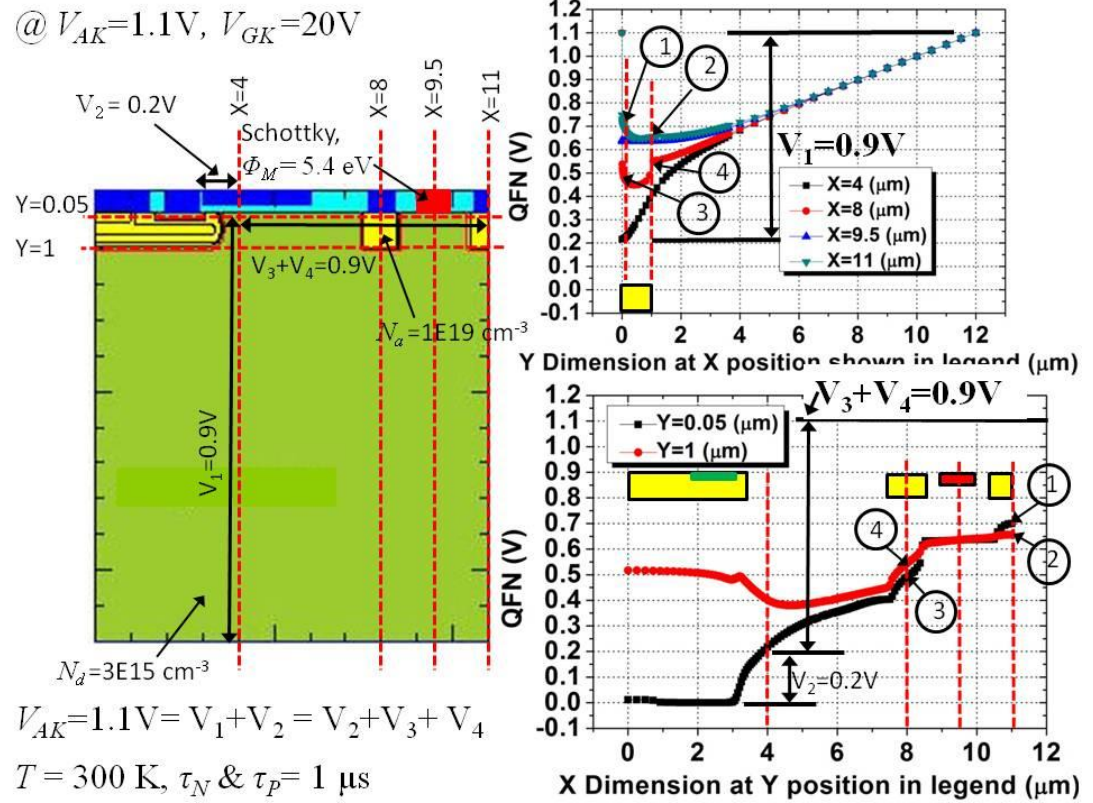


Figure 5.21. Examination of the quasi Fermi potential for electrons at the point of bipolar start up ($V_{AK}=1.1 \text{ V}$).

From figure 5.21 it can be seen that the Schottky has the effect of maintaining bias across the P+ to N- junction of D_2 and D_1 , but recombination is only occurring in D_1 , the closest P-Anode to the lateral drift region forming the PiN diode. In unipolar mode the parallel paths to drain from Node 1 (forming V_1 and V_3+V_4) are equal in terms of volt drop as predicted by the equivalent circuits of figure 5.7 and 5.20. As can be seen from figure 5.22 it is the length of the PiN drift region (given by W_N , where $W_N=W_B$) that is critical to

the resultant potential drop across the N-Drift region which then influences the bipolar start up voltage (V_i) of the injector.

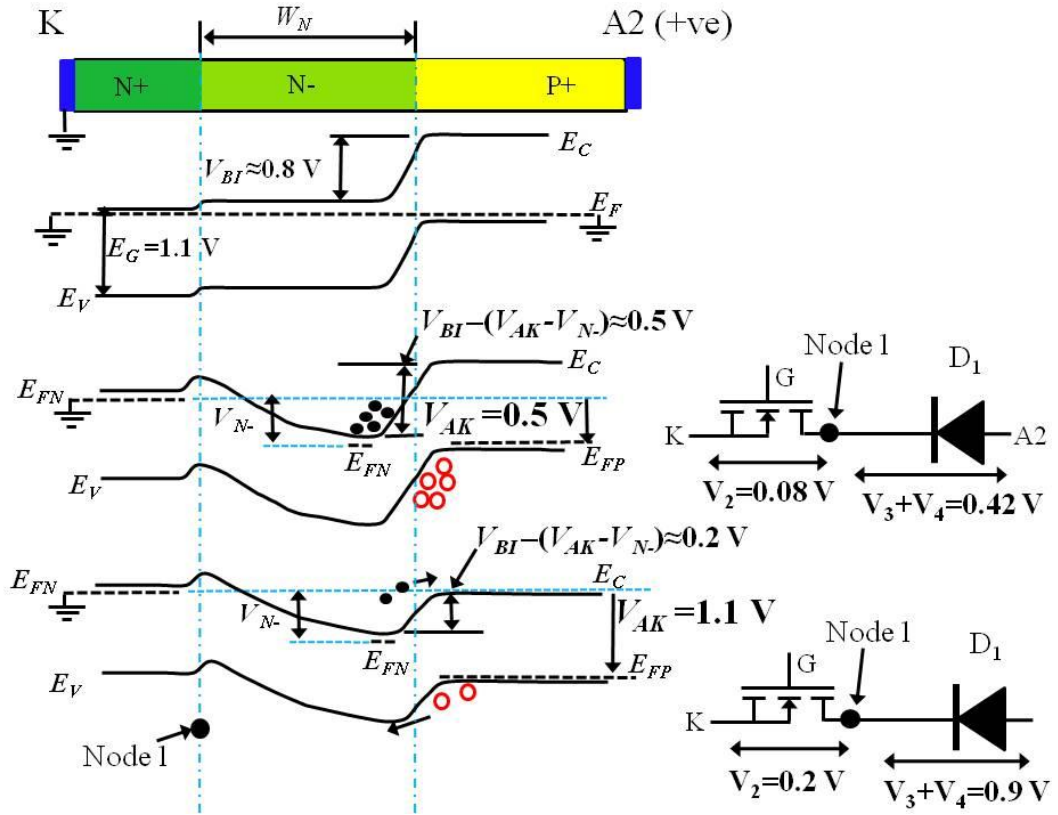


Figure 5.22. Energy band diagrams for the PiN diode for increasing bias (V_{AK}).

5.6 Comparison of lateral injector structures in bipolar mode

The means of achieving sufficient forward bias across laterally placed P-Anode injector, as described section 5.5 is common to all the lateral injector types described in this section.

However, the type of injector structure causes subtle changes in the resultant voltage (V_{EB}) developed across the P-Anode to N- junction of the lateral PiN diode (or emitter to base junction of the PNP BJT). These subtleties become apparent in bipolar mode and will be investigated by the use of two different structures:-

- 1) Merged Schottky contact injector with varied metal work function (Φ_M)
- 2) Solid P-Anode injector

These will again be compared to the VDMOSFET resulting from chapter 3. The resulting structure of each of the above laterally injected devices is shown in figure 5.23. For each

structure the equivalent circuit will be provided in terms of the electron current flow to assist in the description of the resultant P-Anode (or emitter-base) biasing. The resultant hole concentrations and developed voltage across each element of the equivalent circuit will also be provided.

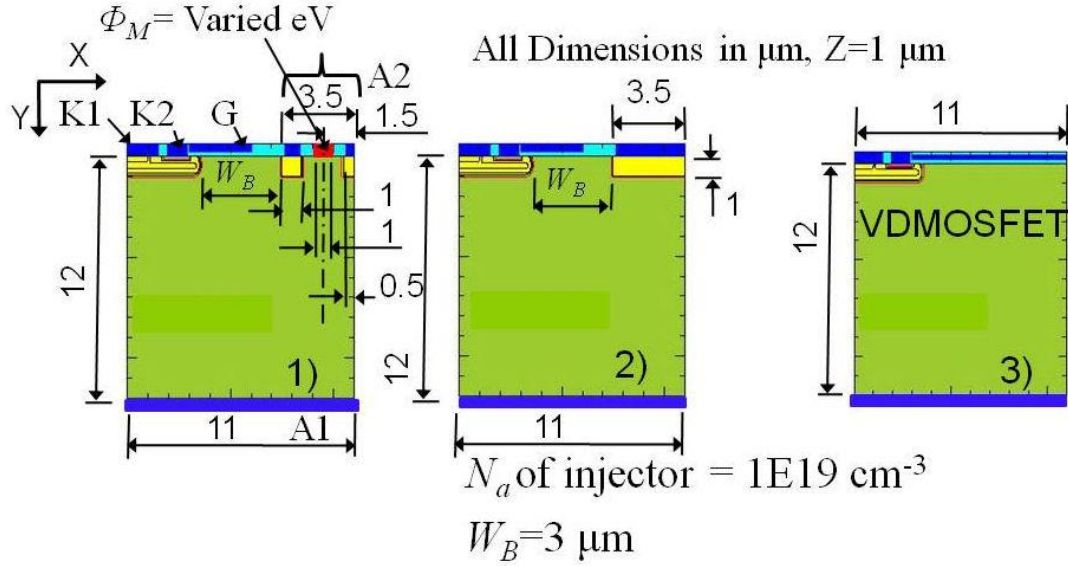


Figure 5.23. Three alternative lateral injector structures trialled: 1) Merged anode/contact with varied Φ_M ; 2) “Solid” P-Anode- no merged contact ; 3) VDMOSFET.

A comparison of I-V characteristics for each of the lateral injector structures is shown in figure 5.24 as compared to the optimised VDMOSFET resulting from chapter 3. The resultant I-V characteristics show the change in total hybrid anode current with increase in terminal bias (V_{AK}) at a fixed gate voltage of $V_{GK}=20 \text{ V}$. As is apparent from these plots, the bipolar start up point is consistent at $V_i=V_{AK}= 1.1 \text{ V}$ due to the fixed N-Drift distance (W_N) as explained in section 5.5. In bipolar mode the structure with the highest metal work function ($\Phi_M=5.4 \text{ eV}$ as related to PtSi) is almost identical to the structure with the solid P-Anode. However, in bipolar mode the slope of the dI_A/dV_{AK} is slightly lower for the merged injector structure. This is due to the Schottky starting to conduct only after bipolar start up due to the increase in carriers within the PNP base region as shown in figure 5.25.

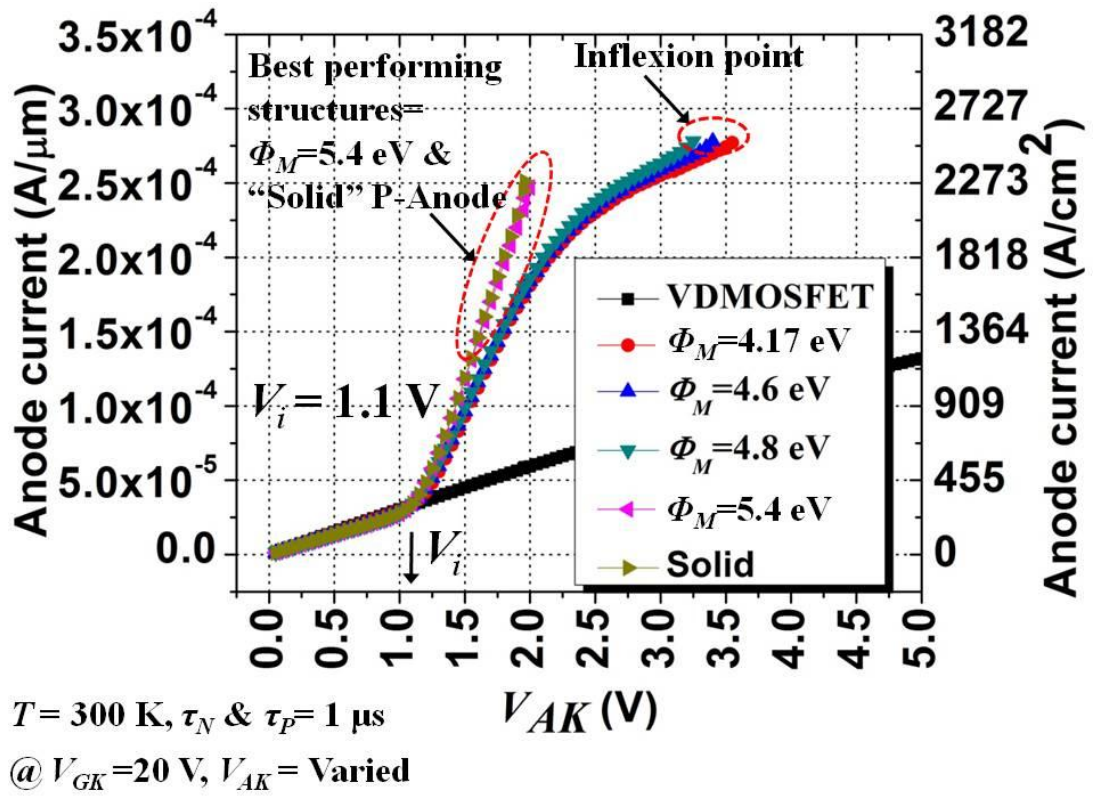


Figure 5.24. A comparison of I-V characteristics of the structures from figure 5.24.

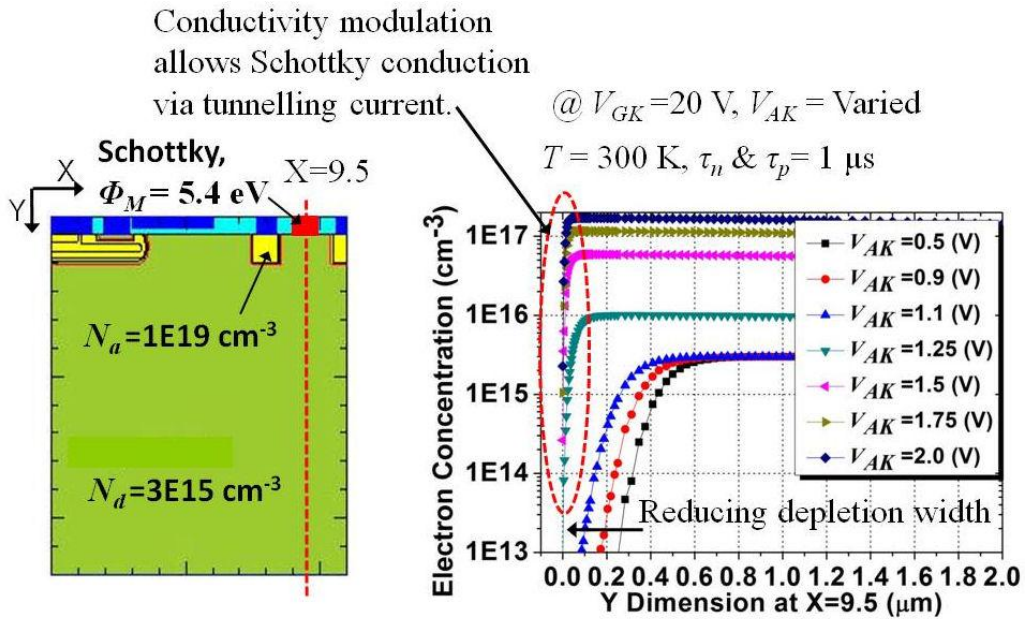


Figure 5.25. Electron concentration at the Schottky contact allowing current flow via Thermionic field emission and potentially via tunnelling through the thin depletion width.

As described by Rhoderick[22] then conduction over the Schottky barrier begins at around $V_{AK}=1.25V$. After the Schottky conducts then fewer of the available electrons were available to form $I_{diff,E}$ into the emitter of the PNP BJT than when compared to the structure with a solid emitter and so the hole current into the base ($I_{diff,B}$) was proportionally reduced. The effect of the variance in metal work function of the Schottky contact was now required. In addition the point of inflexion (as shown in figure 5.24), which altered due to metal work function in terms of V_{AK} , also required explanation.

5.7 Effect of metal work function in the laterally placed injector

The collection of I-V characteristics for the merged Schottky contact injector as the metal work function (Φ_M) of the Schottky contact is varied is shown in figure 5.26. The definition of the contact descriptions used in figure 5.26 is shown in figure 5.27.

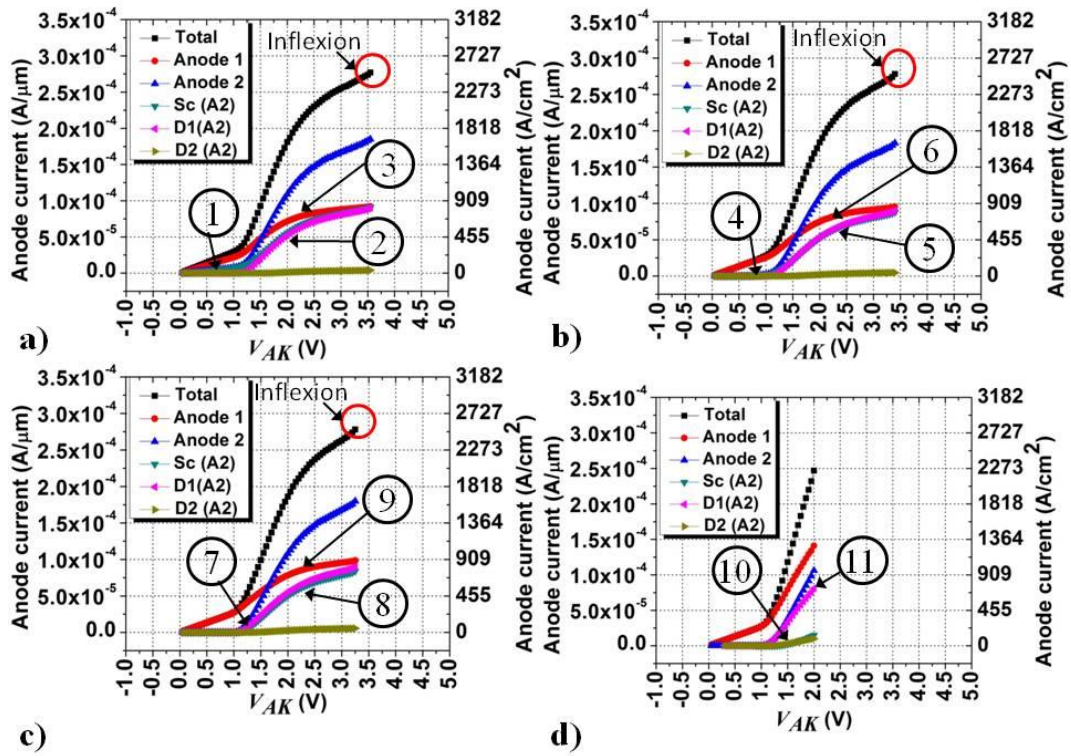


Figure 5.26. Comparison of I-V characteristic with different metal work functions: a) $\Phi_M=4.10$; b) $\Phi_M=4.6$; c) $\Phi_M=4.8$, and d) $\Phi_M=5.4$.

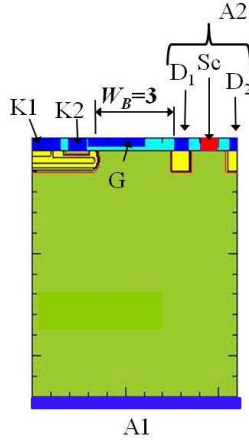


Figure 5.27. Contact definitions to accompany figure 5.26.

Position (1) in figure 5.26 a) shows the conduction via the Ohmic contact ($\Phi_M = 4.10$ eV), in this case conduction via ‘Sc’ starts immediately as there is no potential barrier to overcome. The position of V_i however, does not change (as described in section 5.5), but in bipolar mode the electron current share of $I_{diff,E}$ to D_1 is much reduced as the available current from the MOS channel is split between A_1 , D_1 , and Sc. Of all the other variations in Φ_M , Sc in this case takes the largest share relative to D_1 as can be seen at position (2) as compared to positions (5), (8) and (10) as Φ_M is progressively increased. Position (3) in figure 5.26 a) shows the point at which anode 1 (A_1) saturates indicating when the MOS channel reaches its maximum electron current due to the geometry and inversion level, (in this case $V_{GK} = 20$ V).

As Φ_M is progressively increased in figures 5.26 b) through to d), positions (4), (7) and (10) then the Schottky conduction point increases in terms of terminal bias V_{AK} . The effect is to allow a greater ($I_{diff,E}$) electron current to the P-Anode, hence D_1 increases providing a larger total current via A_2 . Only with the highest work function ($\Phi_M = 5.4$ eV) as shown in figure 5.26 d) is the Schottky conduction starting after that of the bipolar conduction. The current drain via the Schottky is also reduced when compared to that of the lower work function Schottky contacts, hence even more electron current ($I_{diff,E}$) is available to the P-Anode and reflects in the larger current via D_1 , position (11).

The point of inflexion is controlled by the hole current density flowing through the P-body to K1. This is most certainly the point at which the N+ emitter of the parasitic NPN BJT biases on as indicated by the consistent D_1 current level at which the point of inflexion occurs. As shown in figure 5.26 the variation in the terminal bias (V_{AK}) at which the inflexion occurs, as Φ_M is changed, is dependent upon the point at which the current D_1 reaches the hole current density level at which the parasitic NPN activates. Only in figure 5.26 d) with $\Phi_M=5.4$ does the D_1 current level fail to reach the NPN activation current level. It is also the only I-V characteristic in which the current via anode 1 (A1) is larger than that flowing through anode 2 (A2). This indicates that when using the Schottky with $\Phi_M=5.4$ eV the MOS channel would reach its upper electron supply limit prior to the limitation of the electron current share $I_{diff,E}$ to the PNP emitter (D_1), which in turn limits the hole injection and hence the level of conductivity modulation achieved in the PNP BJT base. At $V_{AK}=2.0$ V the electron current via A1 had not yet saturated in figure 5.26 d). The power density for the hybrid with characteristic at a current density of 2000 A/cm^2 at $V_{AK}=2 \text{ V}$ would be 4 kW/cm^2 and yet the NPN BJT had not yet biased on indicating that the device would probably ‘expire’ for thermal reasons before the parasitic NPN BJT had biased on.

The conduction paths within the hybrid operating in bipolar mode are shown in figure 5.28. The effect of decreasing the metal work function of the Schottky conduction path is to decrease the share of electron current to terminal A1, the emitter of the PNP BJT and to support any recombination within the base. The electron current available to the emitter ($I_{diff,E}$) limits the injection of holes into the base. If the hole concentration within the base region of the hybrid with the Ohmic contact is compared to that of the contact with metal work function of $\Phi_M=5.4$, as shown in figure 5.29, then higher electron ‘drain’ via the Ohmic contact as seen in figure 5.26 clearly results in the attainment of a peak hole concentration of $p_n = 6 \times 10^{16} \text{ cm}^{-3}$ at $V_{AK} \Rightarrow 2 \text{ V}$ remaining the same despite further increase in V_{AK} , whereas with a $\Phi_M=5.4$ eV contact then a higher peak of $7 \times 10^{16} \text{ cm}^{-3}$ is reached at $V_{AK}=2 \text{ V}$ and still rising sharply.

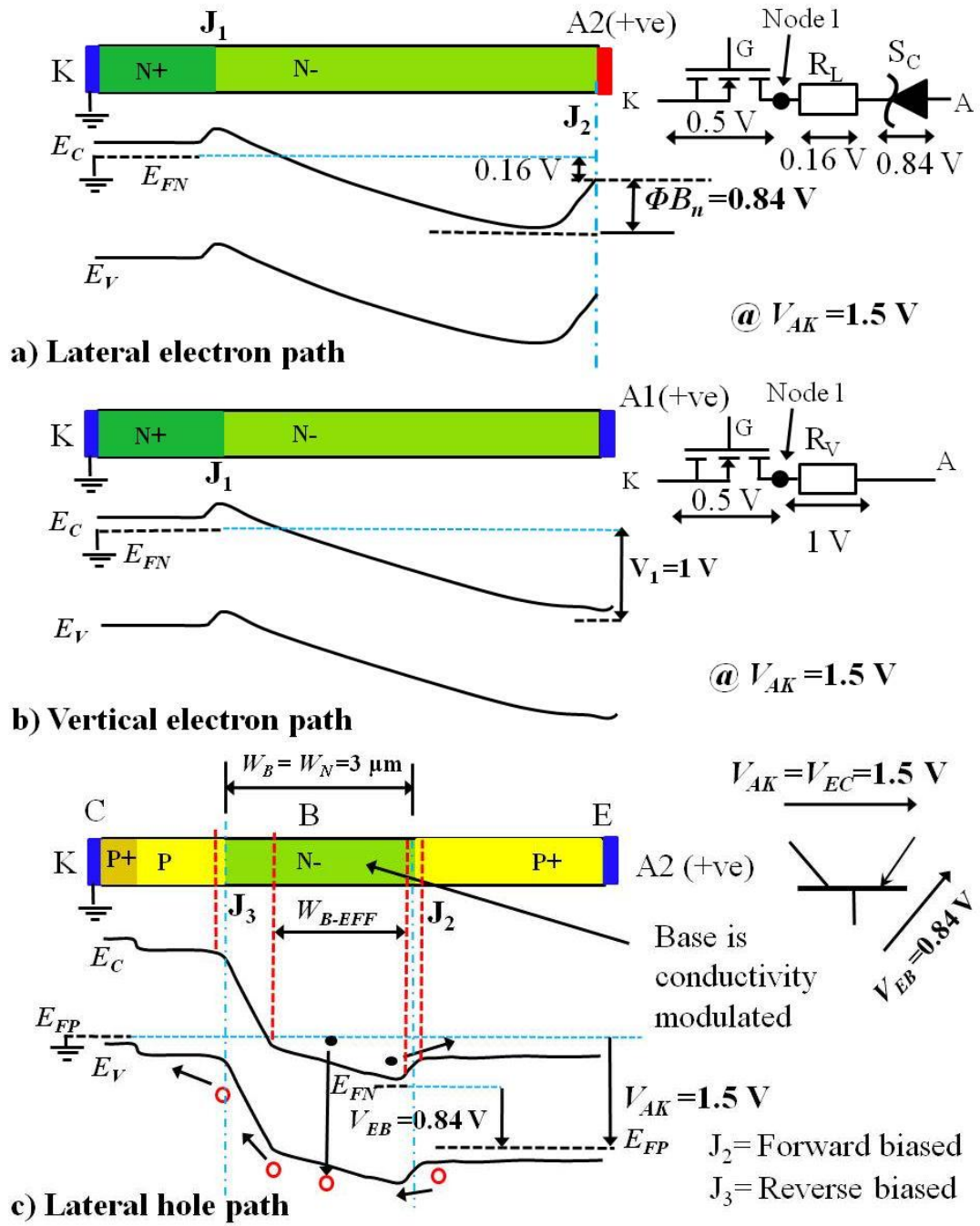


Figure 5.28. Energy band diagrams of the various conduction paths through the hybrid in bipolar mode at $V_{AK}=1.5$ V.

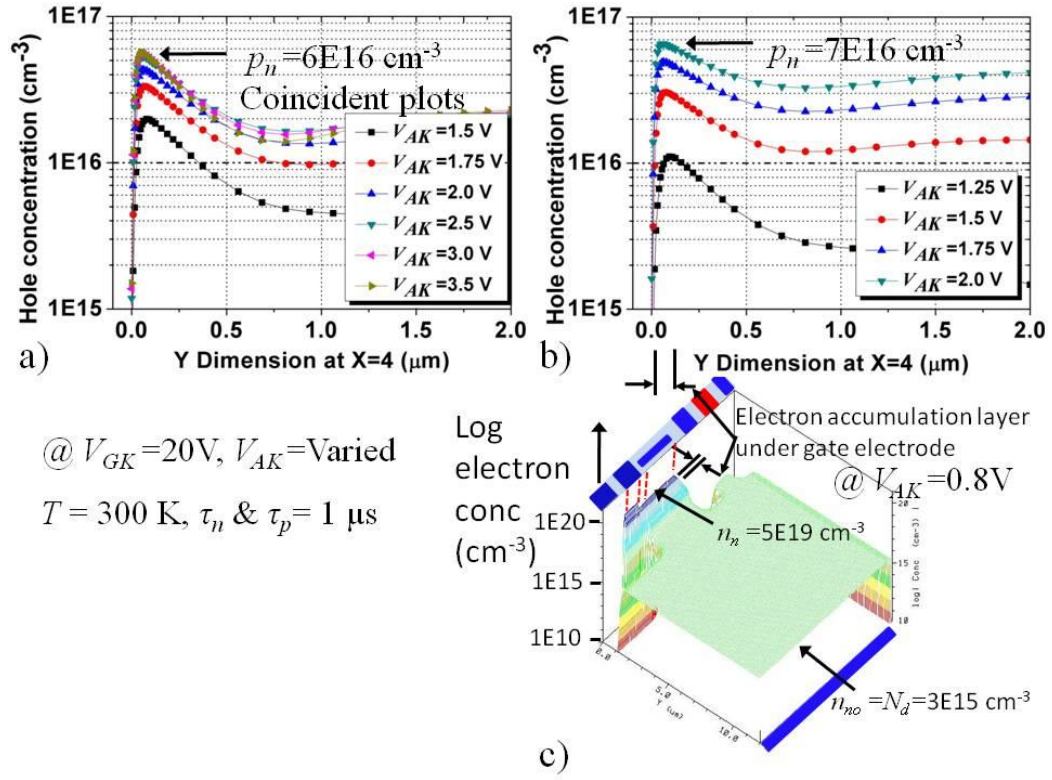


Figure 5.29. Resultant hole concentration at $Y=4$ (μm) for a) injector with Ohmic contact, b) injector with $\Phi_M=5.4$ eV, as compared with c) plot of electron concentration showing MOS accumulation effect.

From equation 5.8 then the base to emitter voltage (V_{EB}) is directly linked to the carrier concentration achieved in the base region. The voltages (as defined in figure 5.20) developed within the hybrid structure with $\Phi_M=5.4$ eV, in bipolar mode (with V_{AK} increased from 1.1 to 2.0 V) are shown in the plot of QFN shown in figure 5.30. For clarity the voltages relating to V_1 , V_2 , $V_3=V_{EB}$ & V_4 are tabulated and shown in table 5.1 below, but figure 5.30 shows the relationship between these voltages.

At the other extreme of Sc where $\Phi_M=4.10$ eV (forming an Ohmic contact) then the tabulated voltages developed within the structure as taken from the QFN results with increase V_{AK} are shown in table 5.2. As described in section 5.5 the bipolar start up voltage is dependent upon $W_N=W_B$ and is consistent regardless of the value of Φ_M . However, the internal voltage distribution in both unipolar and bipolar mode is very different and shown in table 5.2. Crucially at the bipolar start up voltage where $V_{AK}=V_i=1.1$ V, then $V_4 = V_N = 0.222$ V for the Ohmic contact injector, whereas for the Schottky contact injector with Φ_M

=5.4 eV it was 0.186 V. In the Ohmic contact hybrid the effect on V_3 (V_{EB}) therefore is a continuous fixed offset of approximately 0.045 V which reduces the hole injection level as per equation 5.4 for the injected hole current level into the base from the emitter ($I_{diff,B}$).

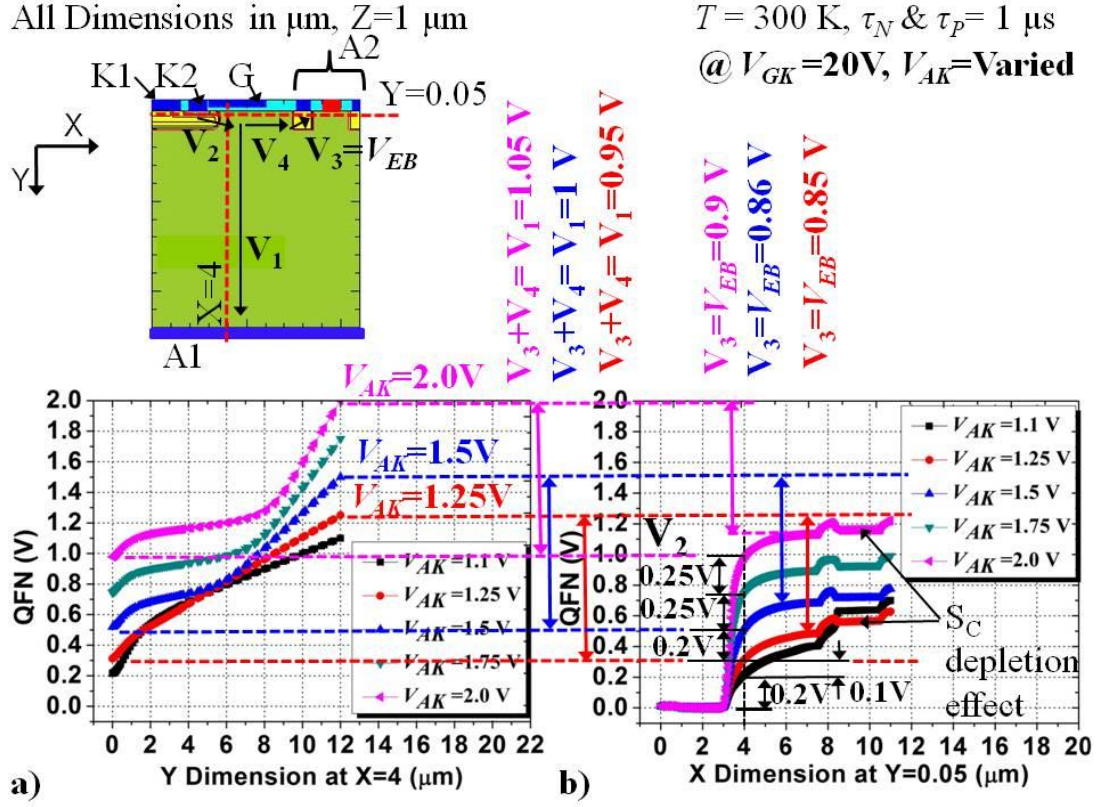


Figure 5.30. QFN plot at a) $X=4$ and b) $Y=0.05 \mu\text{m}$ showing effect on developed voltage within the merged Schottky injected structure as V_{AK} is increased.

The resultant plot of V_{EB} against V_{AK} shown in figure 5.31 presents the comparison of the hybrid structures with $\Phi_M=4.1$ & 5.4 against that of the solid P-Anode. The plot for the structure with $\Phi_M=5.4 \text{ eV}$ is identical to that of the solid P-Anode with the exception that the P-Anode incurs the turn on of the parasitic NPN BJT at $V_{AK}=1.96 \text{ V}$ as indicated by the increase in V_{EB} as caused by the resultant increase in carrier concentration as per equation 5.8 which follows the sudden availability of additional electrons flowing to the emitter ($I_{diff,E}$). The offset in V_{EB} between the lateral structures with lowest and highest work function (Φ_M) is clearly evident from figure 5.31.

V_{AK}	V_1	V_2	$V_3=V_{EB}$	$V_4=V_{N-}$
0.5	0.492	0.008	0.332	0.16
0.8	0.659	0.141	0.521	0.138
0.9	0.74	0.16	0.581	0.159
1	0.818	0.182	0.639	0.179
1.1	0.883	0.217	0.697	0.186
1.25	0.936	0.314	0.766	0.17
1.5	0.98	0.52	0.82	0.16
1.75	1.003	0.747	0.85	0.153
2	1.02	0.98	0.87	0.15

Table 5.1. Voltages as defined in the equivalent circuit using a merged Schottky contact injector with $\Phi_M=5.4$ eV.

V_{AK}	V_1	V_2	$V_3=V_{EB}$	$V_4=V_{N-}$
0.5	0.404	0.096	0.314	0.09
0.8	0.644	0.156	0.492	0.152
0.9	0.724	0.176	0.548	0.176
1	0.802	0.198	0.6	0.202
1.1	0.875	0.225	0.653	0.222
1.25	0.953	0.297	0.726	0.227
1.5	1.006	0.494	0.793	0.213
1.75	1.036	0.714	0.822	0.214
2	1.057	0.943	0.838	0.219
2.5	1.09	1.41	0.86	0.23
3	1.11	1.89	0.86	0.25
3.5	1.13	2.37	0.86	0.27

Table 5.2. Voltages as defined in the equivalent circuit using a merged Ohmic contact injector.

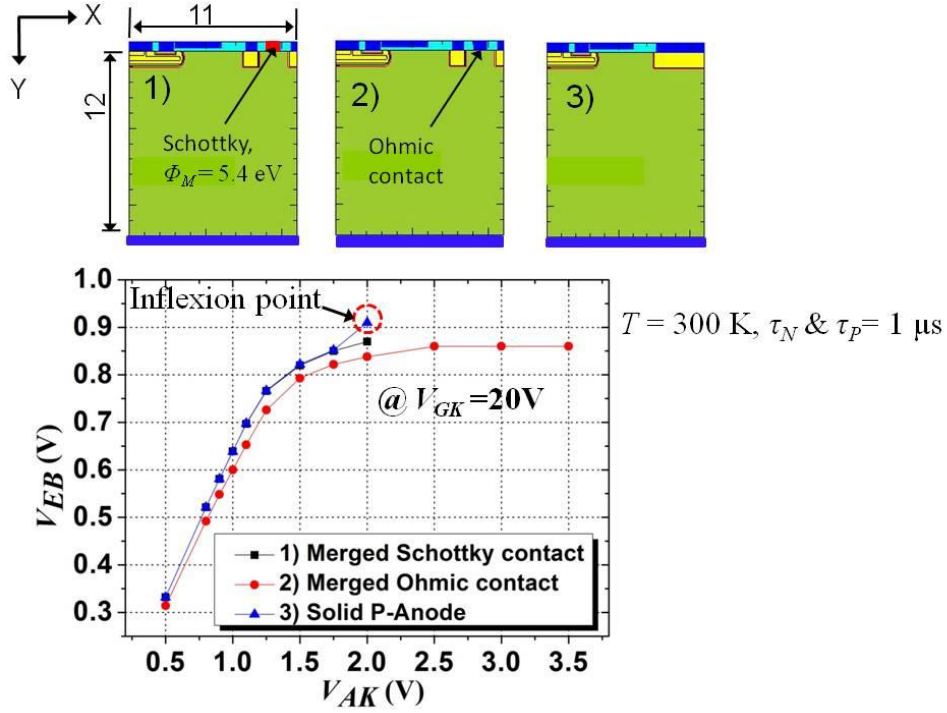


Figure 5.31. Plot of V_{EB} at increasing levels of V_{AK} for different structures of hybrid VDMOSFET as indicated.

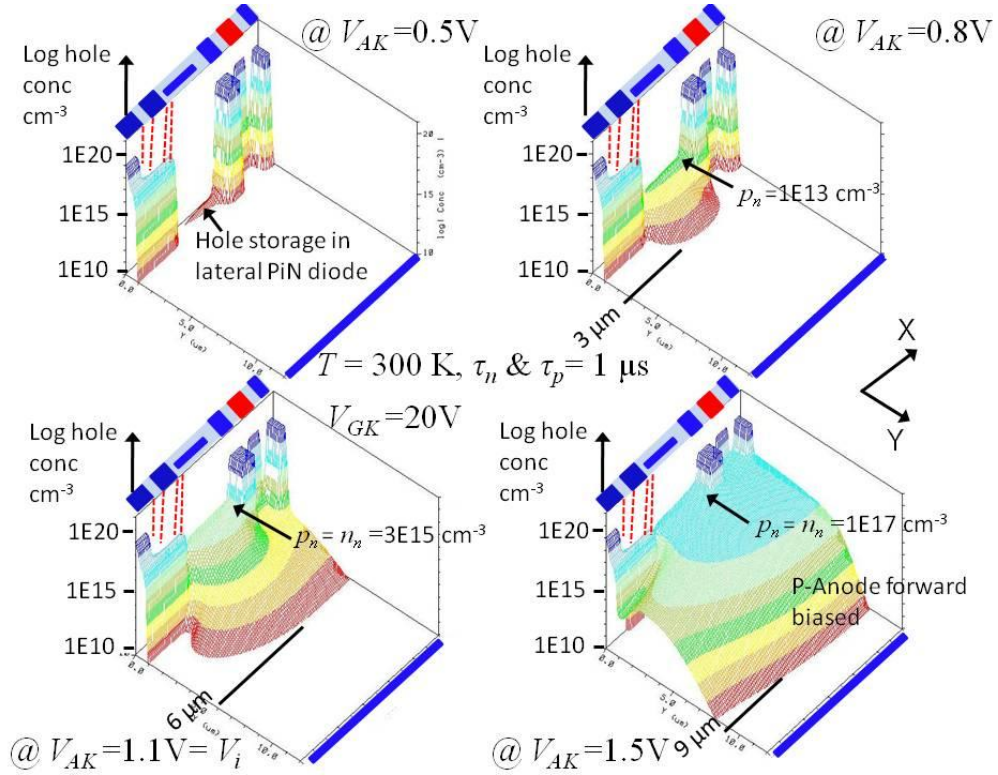


Figure 5.32. Resultant hole concentration within the lateral structure of the injected hybrid with a 3.5 μm long injector ($\Phi_M = 5.4$ eV) at various increments of V_{AK} bias.

The hole concentration achieved as a result of the using the contact with metal work function of $\Phi_M=5.4$ eV, which therefore benefited from the highest electron current share to the emitter ($I_{Diff,E}$), is shown in the series of three dimensional plots as terminal bias is increased. The hole concentration plots are shown in figure 5.32. From table 5.1, figure 5.31 and the hole concentration of figure 5.32 then clearly the emitter to base junction does not de-bias (displaying a reduction in V_{EB}) as a result of conductivity modulation of the PNP BJT base. The value of V_{EB} however, does peak at a maximum value limited by the electron current into the emitter ($I_{diff,E}$) which in turn limits the hole concentration and hence the value of V_{EB} via equation 5.8. In the laterally injected hybrid with metal work function $\Phi_M=5.4$ eV then V_{EB} is prevented from rising higher than the built in potential of the Schottky barrier.

5.8 Achieved blocking voltage of the laterally injected VDMOSFET

The blocking voltage of the vertically injected structure was simulated to be 116 V with drift length of 11 μm and N-Drift doping concentration of $3\text{E}15\text{ cm}^{-3}$ as shown in figure 5.33. In the vertically injected hybrid the BV performance of the P-Anode to N- junction is dominated by the donor concentration (N_d), as per and IGBT structure, Baliga[21], where the blocking voltage can be calculated as per equation 5.12 (Grove[18]). The lateral structure however, requires that in addition the lateral drift width (W_N) is also considered. This is due to the depletion extent from the reverse biased P-body to N-Drift junction (as calculated using equation 5.13, Grove[18]), which may meet that of the forward biased injector junction. Therefore the laterally injected design requires that $W_N > W_D$ at the targeted blocking voltage (BV). If the depletion regions meet then uncontrolled current will flow between cathode to anode 2 described as ‘punch through’ as related to a Bipolar Junction Transistor (BJT), Grove[18], Sze[24].

$$BV_{P+toN-} = \frac{K_s \epsilon_o (\epsilon_{CRIT})^2}{2qN_d} \quad (5.12)$$

$$W_D = \frac{2K_S \epsilon_O (V_{AK})^2}{qN_d} \quad (5.13)$$

In this case a blocking voltage of ≈ 120 V was targeted as achieved by the VDMOSFET resulting from the work of chapter 3. For the laterally injected structure with $W_B = 3 \mu\text{m}$, half cell width = $11 \mu\text{m}$ as demonstrated in this chapter, then the blocking voltage was simulated using $V_{GK} = 0$ V, with V_{AK} stepped at 1 V increments. The results are shown in figure 5.34, which clearly demonstrate punch-through. The lateral injector therefore requires the distance W_B to be increased in order to realise the targeted BV. The impact of changing the distance on the bipolar start up voltage (V_i), and the gain of the PNP transistor, required investigation if the lateral injector idea could be utilised.

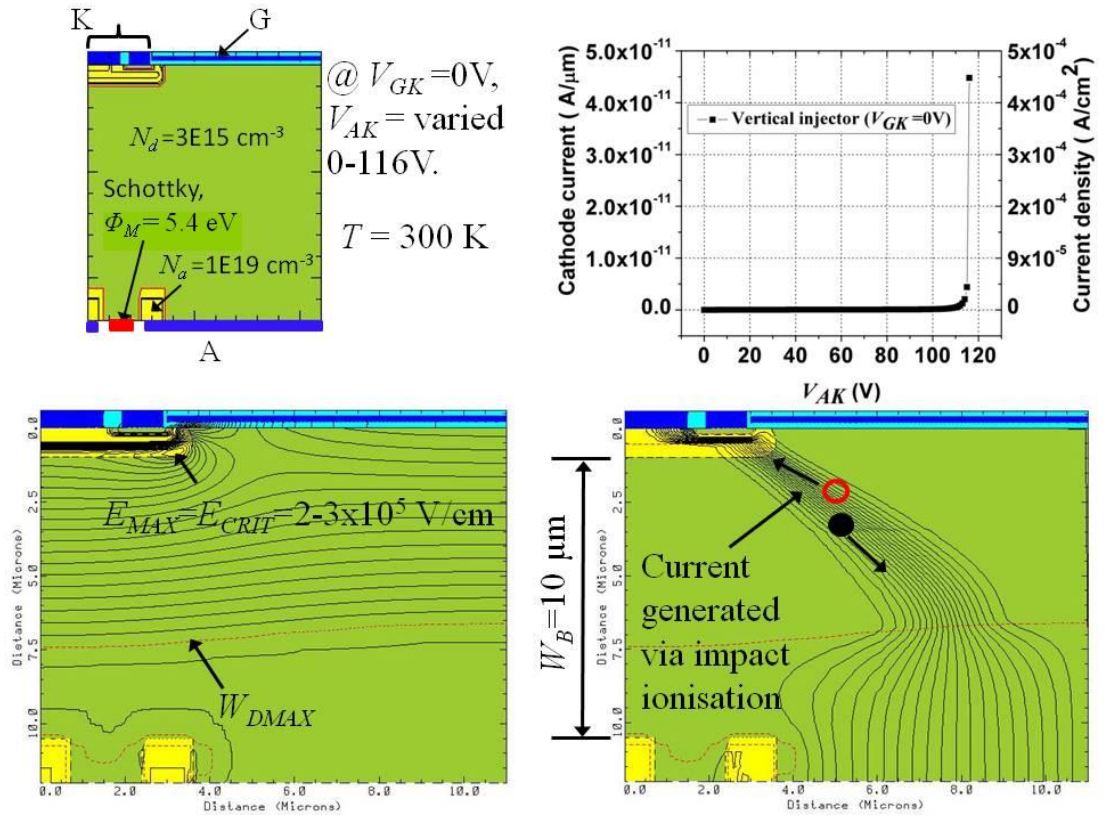


Figure 5.33. Simulated result of the vertically injected structure to determine the BV.

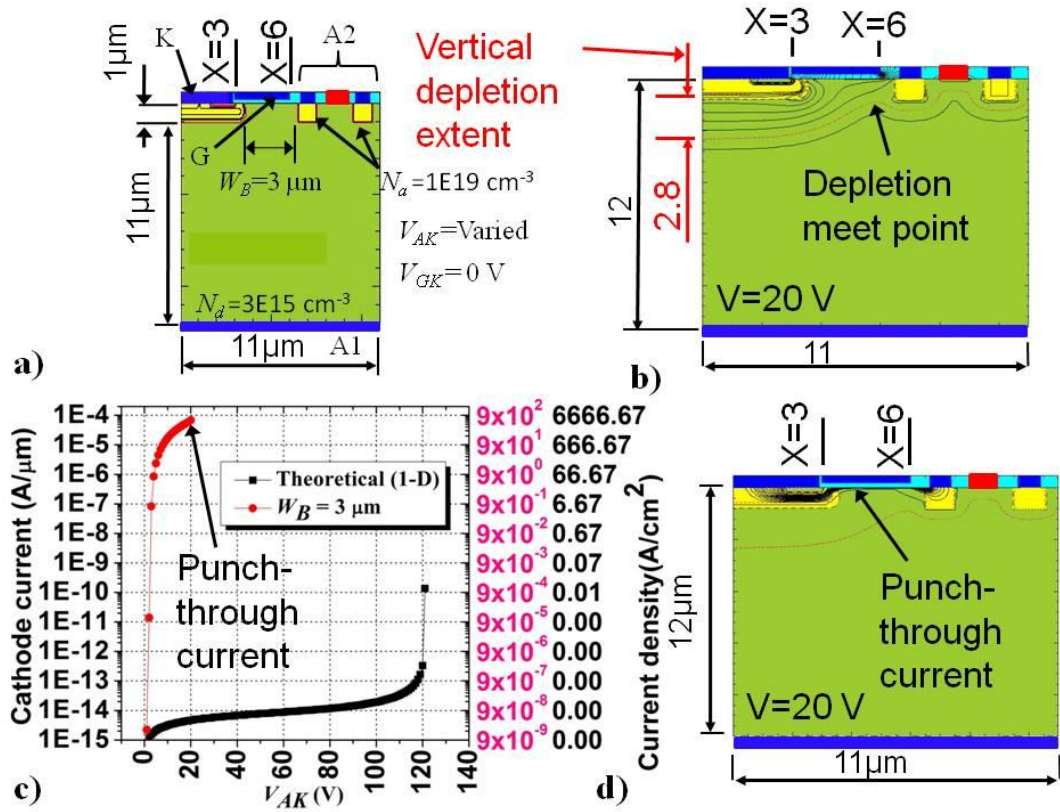


Figure 5.34. Blocking voltage result for hybrid with small lateral drift width (W_N).

5.9 Summary of lateral and vertical hybrid VDMOSFET structures

Within this chapter the state of the art injected MOS gated structures were summarised and a figure of merit performance plot was provided in terms of BV and $R_{(ON,SP)}$, as shown in figure 5.2. With reference to figure 5.2 (with the exception of the work of Weber[16] on which Reynes[9] based his injected VDMOSFET) then of the structures reviewed only the work of Chow[2] achieved significant bipolar conduction, unfortunately this device suffered from high $R_{(ON,SP)}$ due to the need to use of external bias resistors.

A direct comparison of the lateral and vertical structures with a gate bias of $V_{GK} = 20 \text{ V}$ and use of a merged injector utilising a Schottky contact with a metal work function of $\Phi_M = 4.8 \text{ eV}$ is shown in figure 5.35. The bipolar start up of the vertical structure with a 6 μm long injector is at $V_{AK} \approx 2 \text{ V}$, but for the lateral structure with a reduced base width ($W_B = 3 \mu\text{m}$ as opposed to $W_B = 10 \mu\text{m}$ for the vertical structure) $V_{AK} = 1.1 \text{ V}$. The effect of the base width therefore is very clear as regards bipolar activation. Unfortunately, the proximity of the emitter to collector in the lateral structure caused a reduction in blocking voltage due to the

occurrence of punch-through. The lateral structure therefore required further optimisation to provide good PNP BJT performance and yet also ensure an improved BV performance.

From figure 5.35 the bipolar start up point (V_i) of the vertical structure could be reduced by increasing the length of the injector structure however, this is detrimental to the unipolar current and causes increased $R_{(ON,SP)}$. Certainly in comparison to the lateral structure the vertical structure will always have an increased $R_{(ON,SP)}$. The $R_{(ON,SP)}$ for the lateral structure is almost identical to the VDMOSFET with the exception of the recombination current into the P-Anode (emitter of the PNP BJT) and current via the Schottky which has an increasingly large detrimental effect on $R_{(ON,SP)}$ as the metal work function of the Schottky contact is reduced. The effect of decreasing the Schottky contact work function on the unipolar current of the vertical structure is to increase the bipolar start up voltage (in terms of V_{AK}), but no further impairment of $R_{(ON,SP)}$ occurs. The contact work function could therefore be used to adjust the final design in terms of V_i , without changing the mask set if the vertical device was fabricated.

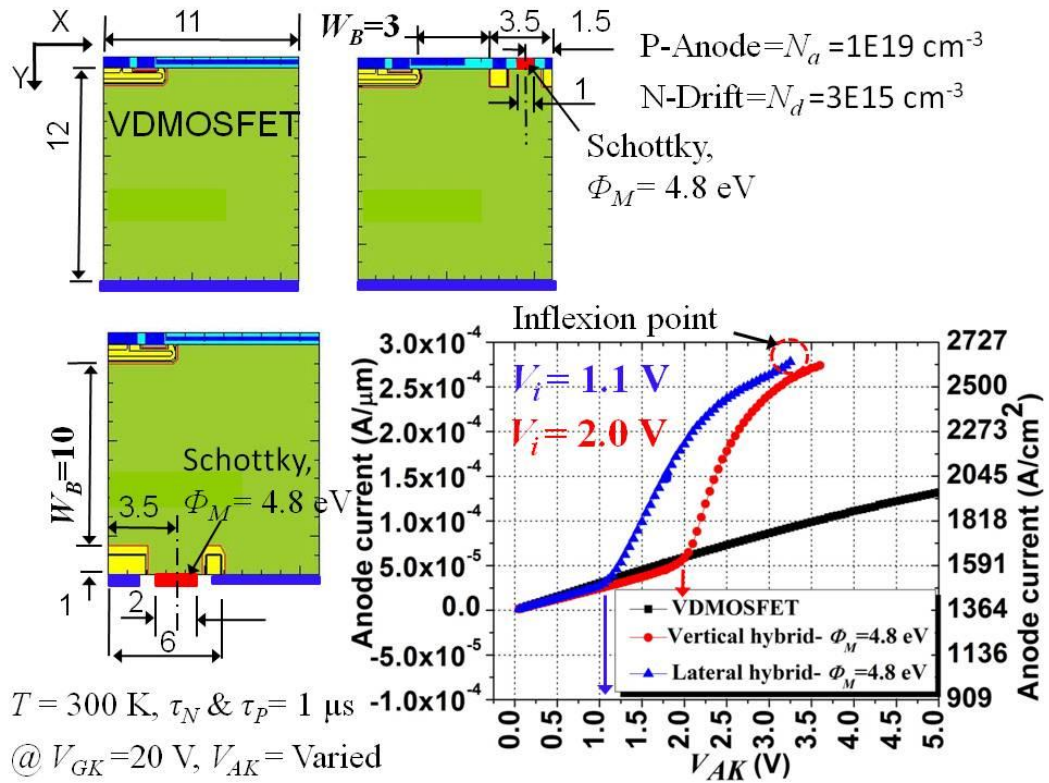


Figure 5.35. Direct comparison of lateral and vertical hybrid structures ($V_{GK} = 20$ V).

The effect of decreasing the Schottky metal work function on the bipolar current of the vertical injector is to reduce the hole injection into the base of the PNP BJT from the emitter, the device saturates in this case due to hole supply deficiency which occurs at lower current levels for lower work functions. The effect in the lateral injector is identical. In both cases with $\Phi_M=5.4$ eV then saturation is caused by the limitations of the inverted MOS channel due to its geometry and gate bias.

Finally, the vertical structure is prone to activation of the parasitic NPN BJT but, it may be easily protected from this occurrence via the use of what have become standard techniques within an IGBT design.

The next aspects of the hybrid device to be investigated were as follows:-

- 1) How could the PNP BJT performance within the lateral device be optimised further, via adjustment of base width (W_B), taking into account the punch through voltage V_{PT} . What is the resulting effect on BV ?
- 2) How does the improved lateral hybrid compare against the vertical hybrid if that remains unchanged?
- 3) Are there any means available to increase V_{EB} levels within the lateral hybrid to improve the PNP BJT performance, if so what are the effects on the unipolar performance?

5.10 References

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Chapter 6 | Optimisation of the laterally injected VDMOSFET

6.0 Introduction

Having determined within chapter 5 that a hybrid MOSFET –IGBT device could be formed either by use of a vertical, or lateral, placed injector to provide a self biased integral PNP Bipolar Junction Transistor (BJT) function in conjunction with the parallel provision of a unipolar electron path from the inverted channel to the anode (biased at $+V_{AK}$). The aim of this chapter is to determine if the laterally injected structure could be optimised in terms of the resultant blocking voltage BV , PNP BJT gain (α) and punch through voltage (V_{PT}), as previously in chapter 5 V_{PT} was $\ll BV$.

Within the vertically injected structure, as the P-body was shielded, these parameters were dictated only by the Vertical N-Drift, or base, region doping (N_d) and PNP BJT base width, W_B (or PiN diode drift length, W_N) as per a standard None Punch-Through (NPT) IGBT structure (see open base transistor breakdown, BV_{CEO} , Baliga[1]). However, in the laterally injected structure the P-body is no longer shielded by an adjacent P-body, the resultant blocking voltage ($BV=BV_{CEO}$) would be reduced relative to the vertical hybrid, of the same N-Drift N_d , due to the electric field (ϵ_{MAX}) at the exposed radius of curvature.

In order to obtain improved PNP BJT performance, the base width (W_B) required to be minimised. The N-Drift length of the lateral PiN (W_N , where $W_N=W_B$) was found in chapter 5 to dictate the start up of bipolar conduction (V_i) in terms of applied terminal bias (V_{AK}). The shorter the base width (W_B) then the lower the start up voltage (V_i). The distance

between the P-body and the P-Anode of the injector was therefore of critical importance to the lateral hybrid design and required work to optimise it in context with the BV . Once the laterally injected device was optimised then a performance comparison could be made between the dc (or static) characteristics of the vertical and laterally injected devices. This work would allow a decision to be made as to which structure gave the best static performance. In chapter 7 the dynamic loss of the device with the best static performance will be evaluated.

6.1 Problem definition

In a VDMOSFET structure protection of the P-body radius of curvature is provided by the adjacent half cell and the use of a continuous gate electrode between them to act as a field plate. Good design practice minimises the lateral distance to minimise the $R_{(ON,SP)}$ of the device as described by Baliga[1]. Considering the electric field then the effects of the P-body radius of curvature in a VDMOSFET in comparison to the one dimensional or theoretical (doping dependant) breakdown is shown in figure 6.1. For a given level of donor concentration in the N-Drift region (in this case $N_d=3E15 \text{ cm}^{-3}$), the one dimensional (theoretical) blocking voltage (BV) and resultant extent of the reverse biased P-N junction (P-body to N-Drift region) depletion region into the N-Drift region of a one sided step junction, W_{DMAX} can be calculated using equations 6.1 and 6.2.

$$BV = \frac{\epsilon_{\max} W_{DMAX}}{2} = \frac{K_s \epsilon_o \epsilon_{\max}^2}{2qN_d} \quad (6.1)$$

$$W_{DMAX} = \left(\frac{2K_s \epsilon_o V_{AK}}{qN_d} \right)^{0.5} \quad (6.2)$$

Where V_{AK} is terminal bias with $V_{GK}=0 \text{ V}$.

The maximum electric field (ϵ_{MAX}) achieved at a given terminal bias (V_{AK}) is given by equation 6.3.

$$\epsilon_{MAX} = \left(\frac{2qN_d V_{AK}}{K_s \epsilon_o} \right)^{0.5} \quad (6.3)$$

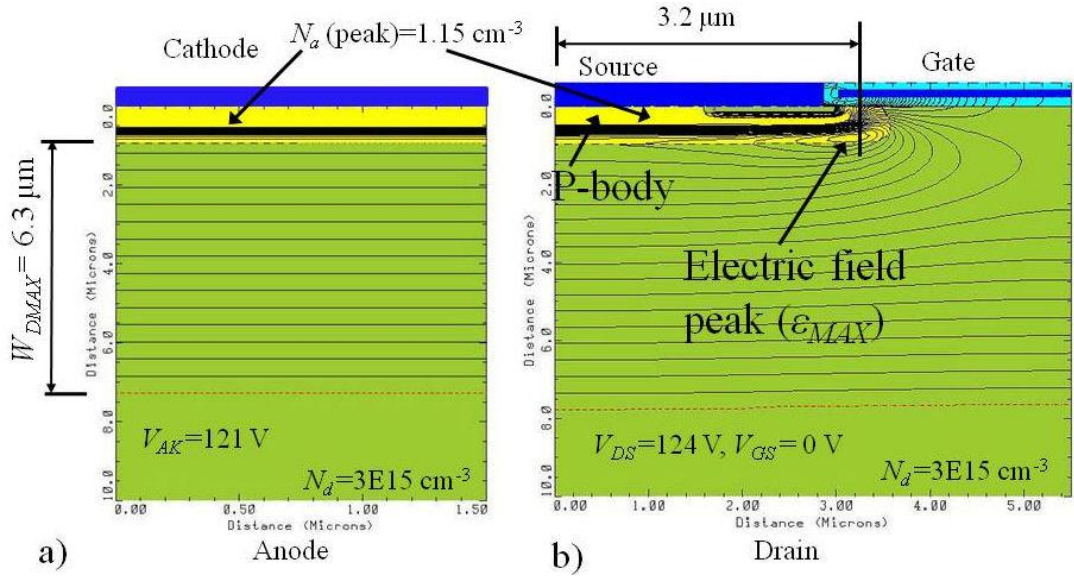


Figure 6.1. Comparison of electric field profile for a) one dimensional structure and b) the two dimensional as optimised VDMOSFET structure.

Through use of equation 6.2 the calculated depletion extent into the N-Drift region (W_{DMAX}) in order to achieve $BV = V_{AK} = 120 V$ was $7.3 \mu m$ with $N_d = 3E15 cm^{-3}$, which assumed uniform acceptor doping (N_a) in the anode, and hence the simulation result of $6.3 \mu m$ was considered valid. In this case, as indicated in figure 6.1, the BV achieved in both structures was approximately the same demonstrating the effectiveness of the shielding from the adjacent P-body. Where avalanche breakdown of the P-body to N-Drift region junction occurs when the electric field maximum (ϵ_{MAX}) is equal to the critical electric field (ϵ_{crit}), (which for silicon $\epsilon_{crit} = 2$ to $3E5 V/cm$). The data used in figure 6.1 resulted from the P-body optimisation work of chapter 3.

If consideration is now given to the laterally injected structure then as shown in figure 6.2 the P-body is no longer protected by any adjacent P-body from a neighbouring half cell as the injector structure (anode 2) is now separating them and this injector is forward biased with respect to the P-body (collector) to N-Drift region (base) junction. The use of a lateral injector therefore causes three issues:-

- 1) There is no longer any protection available from a neighbouring P-body to shield the radius of curvature of the P-body and hence the breakdown voltage is reduced.

- 2) The lateral extent of the depletion from the reverse biased collector to base junction as V_{AK} increases may meet that of the forward biased emitter to base junction and cause punch through (or reach – through). As described by Baliga[1], Yang[2] and Sze[3] this will occur if dimension W_B is too small.
- 3) To ensure the common base gain ($\alpha \approx 1$) within the PNP BJT a reduction in the base width (W_B) is required; this is counter to the needs of issue 2 above.

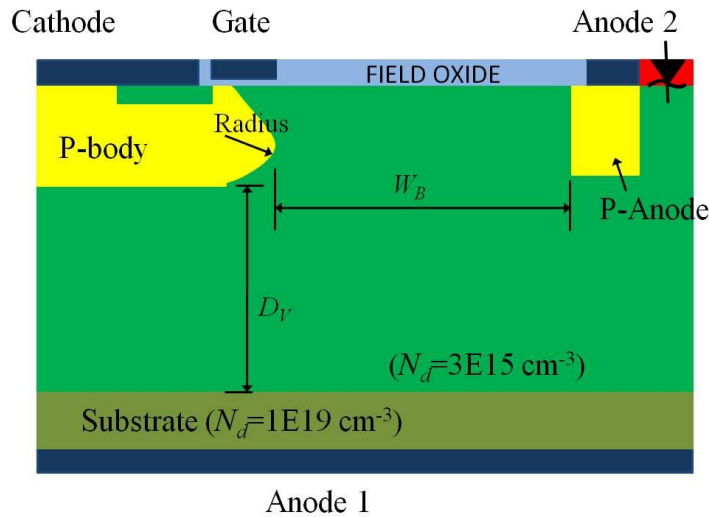


Figure 6.2. Laterally injected hybrid structure showing key distances.

Hence, in the lateral structure of the hybrid device the separation distance (W_B) becomes critical to the design. A demonstration of lateral punch through was provided in figure 5.35 of chapter 5, this figure also shows the associated reduction in BV from that achieved using the equivalent P-body doping in a one dimensional (doping dependant) theoretical device simulation. The causes of punch through current flow can be seen in the band diagram of figure 6.3.

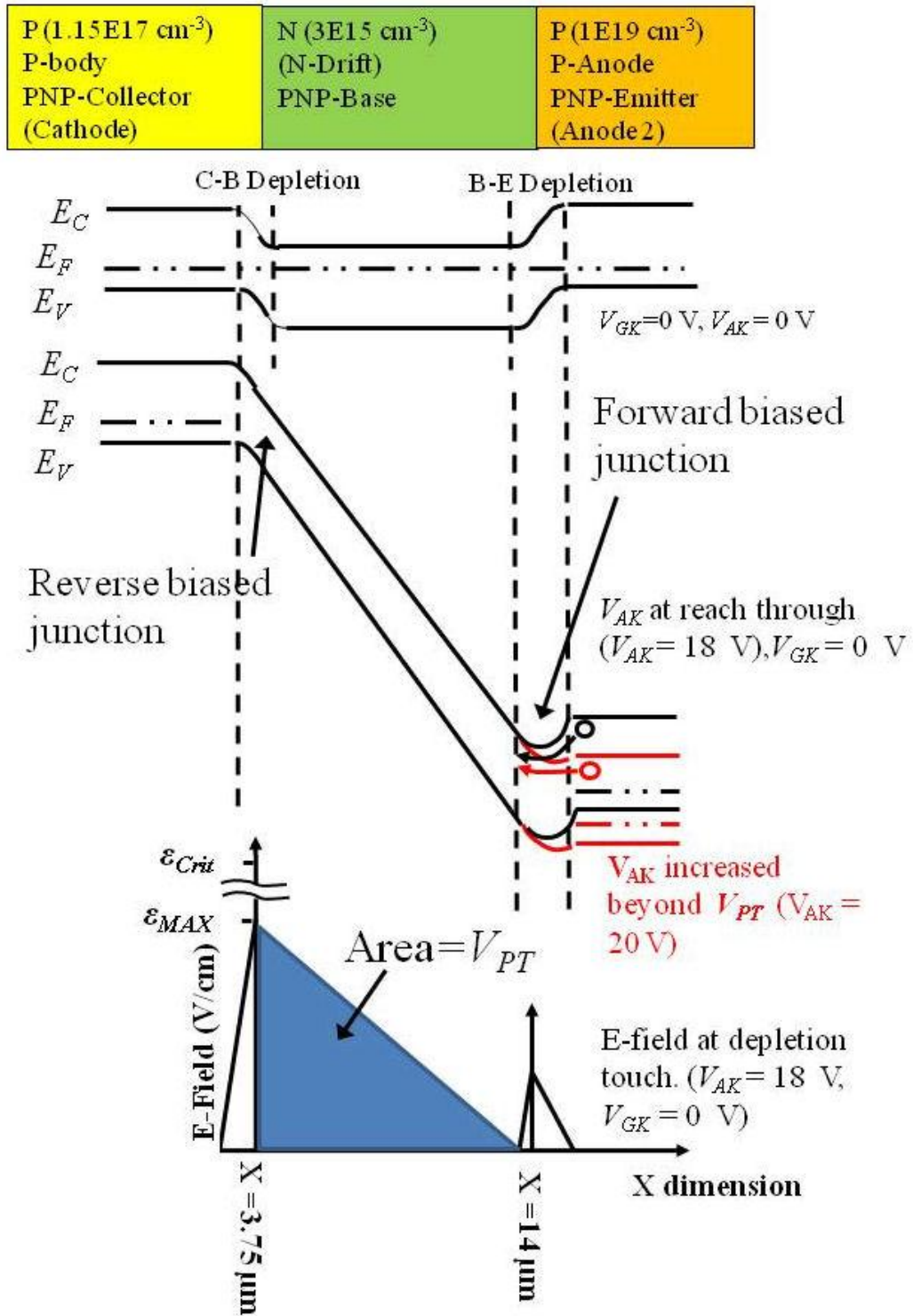


Figure 6.3. Band diagram and electric field plot of the Punch-through mechanism in hybrid device if W_B is too low to support the rated terminal bias (V_{AK}).

6.1.1 Defining the lower limit of base width reduction

The punch through voltage (V_{PT}) or reach through limit was defined by Baliga[1] as per equation 6.4.

$$V_{PT} = \left(\frac{qN_d W_B^2}{2\epsilon_o K_s} \right) \quad (6.4)$$

In optimising the design of a BJT, or the BJT within an NPT-IGBT, then V_{PT} often coincides with the open base transistor breakdown (BV_{CEO}) as described by Baliga[1] and Sze[3]. This is due to the need to reduce both the base doping and width in order to maximise the common emitter gain (β) of the BJT (Blicher[4], Baliga[1]). If the base was highly doped or very wide then obviously the punch through voltage will be high. Similar to the NPT-IGBT, then within the hybrid $V_{PT} \geq BV$, where the BV voltage relates to the avalanche voltage. Rearranging equation 6.4 to provide the minimum W_B to achieve a conservative $V_{PT}=100$ V, then W_B minimum = 6.62 μm if $N_d=3\text{E}15 \text{ cm}^{-3}$ in an NPT-IGBT.

6.1.2 Requirements for highest PNP BJT common base gain

In the last section it was seen that to avoid punch through a high donor concentration in the base region and wide base width were required. Unfortunately, to provide a good PNP BJT performance within the hybrid (maximise the common base gain, α), then the base width (W_B) needs to be minimised according to Grove[5]. With reference to section 5.2.3 in chapter 5, then if W_B is much less than the minority carrier diffusion length in the base (L_{pB}) then this has the effect of reducing the chance of holes recombining with electrons and hence more holes are collected through improvement of the base transport factor (α_T). To minimise the base width it is often necessary to increase the donor concentration of the base in line with equation 6.4, but with the hybrid any increase in N-Drift donor concentration would be detrimental to the vertical VDMOSFET blocking voltage in line with equation 6.1.

Alternatively, the gain (β and α) may be improved by use of an impurity gradient in the base region (with highest doping at the emitter side of the base) as described by Sze [3] and Grove[5]. According to Grove[5] this enables a reduction in base width, but also induces a

small electric field across the base region which enables an element of drift current to assist the diffusion current of holes to the collector. Grove further stated that this improves the transit time (t_{tr}) as shown in equation 6.5 and hence improves the base transport factor (α_T) and increases the cut –off frequency, although this is not specifically of benefit to the sporadic switching events of the SSPC application.

$$t_{tr} = \int_0^{W_B} \frac{dX}{v(X)} \approx \frac{W_B^2}{2D_{pb}} \quad (6.5)$$

Where $dX = v(X)dt$ and v is drift velocity (cm/s) and D_{pb} is the diffusivity of holes in the base.

6.1.3 Summary of base width compromise

To summarise this section the base width required minimisation in order to increase the gain (both α and β), however, in order to avoid punch through prior to BV the base needs to be wide ($V_{PT} = 100$ V a calculated minimum base width limit was $6.63 \mu\text{m}$ using equation 6.4 with $N_d = 3\text{E}15 \text{ cm}^{-3}$). Thus there is a conflict in these requirements which will be explained in the following sections.

6.2 Optimisation of the lateral hybrid device blocking voltage

In this section the optimised lateral hybrid device will be presented which obtained the best compromise as regards the conflict between W_B and V_{PT} as described in the preceding section. In order to achieve this we must study the loss of protection from an adjacent P-body. This description will encompass the reason why the lateral depletion extent is not necessarily identical to the vertical depletion extent due to surface effects such as those from a field plate.

6.2.1 Effect of a field plate on lateral depletion width

A field plate is an extension of the cathode contact across the field oxide of the VDMOSFET device. It can be used to protect the outer periphery of the MOSFET active area, as described by Baliga[1]. Such a structure therefore could therefore be used to protect the exposed radius of curvature resulting from use of the lateral injector structure. Protection is dependent upon

the oxide thickness as described by O'Neil[6] and Baliga[1]. Unfortunately, the use of a field plate has the effect of extending the depletion width to increase the charged volume and hence decrease the level of the maximum electric field (ϵ_{MAX}) achieved at the radius of curvature, but this is counter to the need to reduce W_B in order to increase the gain (α) of the lateral PNP BJT.

To demonstrate the above the effect of using the gate electrode (with $V_{GK}=0$ V) as a field plate was assessed using the various structures shown in figure 6.4. The gate lengths were varied as follows:- a) gate length= $4.75\ \mu\text{m}$, b) gate length = $6.0\ \mu\text{m}$ and finally c) the gate length extended across the entire half cell width. The I-V characteristics and two dimensional electric field contour plots are shown in figures 6.5 and 6.6 respectively. Clearly from figure 6.5 the smaller the gate length then the lower the BV for the structure due to the increasingly exposed radius of curvature. Unfortunately, the longer the gate electrode (field plate) as shown in figure 6.6, the larger the lateral extension of the depletion width, which would result in an increased PNP BJT base width if punch through was to be avoided. As the need was to minimise the base width then the use of a field plate was not possible to protect the radius of curvature.

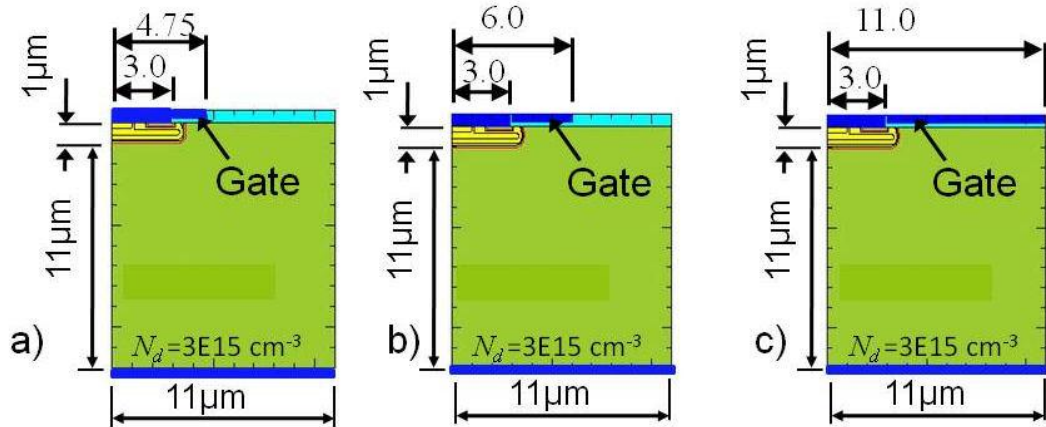


Figure 6.4. The optimised VDMOSFET structure, but half cell width now increased to $11\ \mu\text{m}$ to assess the effect of varying gate length (or field plate length).

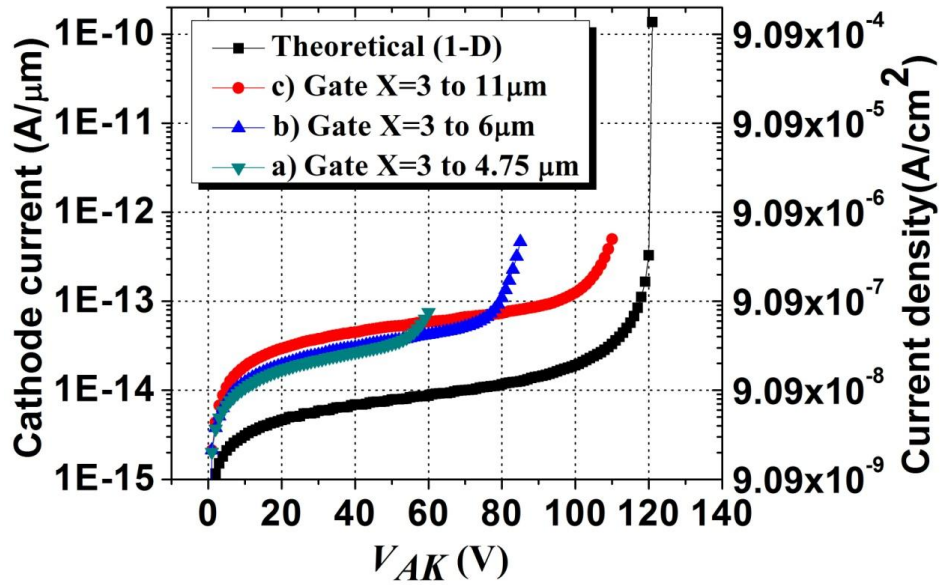


Figure 6.5. Comparison of simulated I-V results of structures detailed in figure 6.4 (with $V_{GK}=0$ V) as compared to doping dependant (1-D) avalanche breakdown.

As demonstrated in figure 6.6 a gate width of reduced length from the half cell width meant that the gate electrode ended abruptly with a sharp corner causing an increased electric field in the thin gate oxide at that point as shown in figure 6.7 a) and b), inducing a high electric field point across the oxide to the gate which in turn caused inversion of the channel causing a coupled current flow and hence reduced BV as shown in figure 6.6. One way to reduce this stress point is to bring the gate electrode up over the field oxide to remove the sharp edge and use the thicker field oxide to reduce the electric field (figure 6.7 d). Unfortunately, this structure type was difficult to replicate in Synopsys Medici without using the Synopsys processing simulator ‘TSUPREM’ [7] so was not simulated. Alternatively, an overlay a field plate from the cathode could be used to protect both the radius of curvature and the sharp end of the gate electrode. Unfortunately, to be effective at reducing the electric field at the gate electrode end the cathode extension plate must extend beyond the gate electrode and therefore has the effect of lengthening the lateral depletion width relative to the vertical depletion width, thus a lateral buffer layer was required to reduce the inevitably large lateral depletion extent.

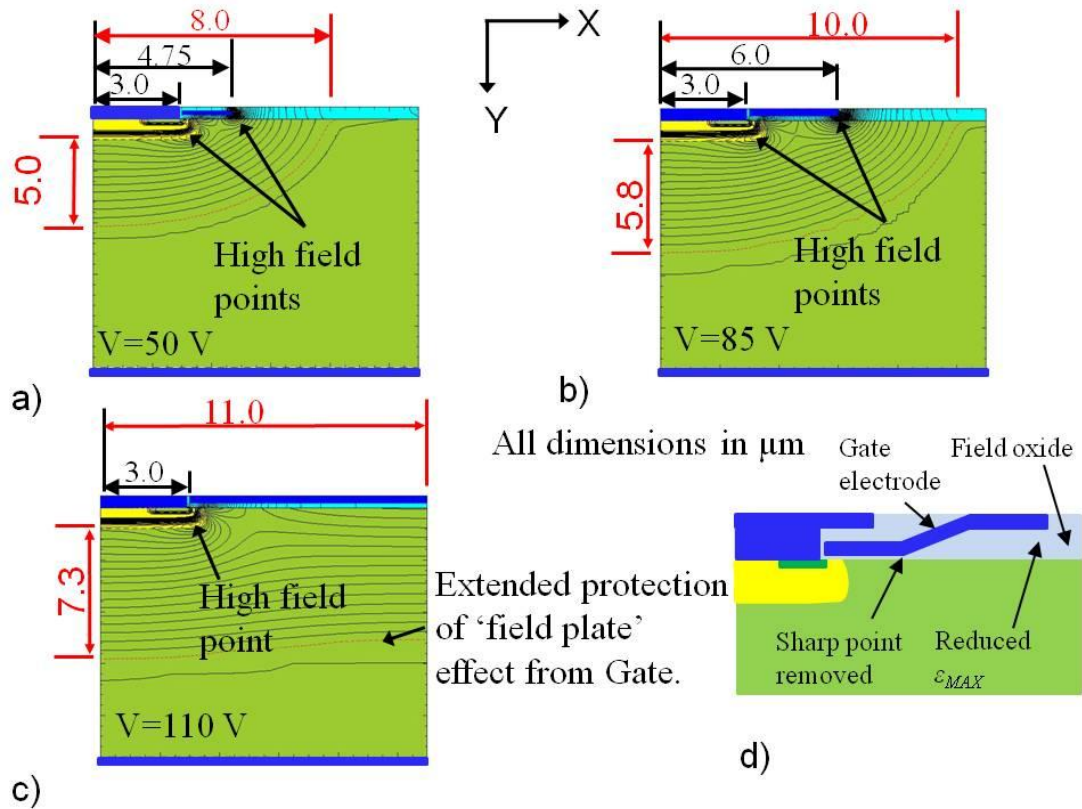


Figure 6.6. Comparison of simulated electric field contours (with $V_{GK}=0$ V); a) thru c) are as related to the various models shown in figure 6.4; d) shows the ideal gate electrode structure to reduce the electric field in the oxide.

6.2.2 Use of a buffer layer to reduce the base width

The conclusion of the literature review of Chapter 2 was that a Non Punch Through IGBT device was the most rugged when compared to that of a Punch Through (PT-IGBT) type, this was due to the predominate use of the drift current transport mechanism in the NPT-IGBT rather than the diffusion mechanism prevalent in the PT IGBT as described by Laska[8]. The PT structure however, provided improved emitter efficiency and a reduced base width therefore provided an increased gain (α) and allowed faster turn off, thus achieved a lower turn off energy (E_{off}). The lower reverse blocking voltage (BV_R) of the PT-IGBT than the symmetrical NPT-IGBT was also of no consequence to the VDMOSFET hybrid due to the body diode effect via anode 1 at the bottom of the device. The benefit of using the DMOS structure rather than UMOS, as regards to the reduced current density

around the channel and hence increased ruggedness as described in chapter 2, however is retained.

The utilisation of a buffer layer within the PT-IGBT therefore has a direct effect on the electric field and extent of the lateral depletion region from the reverse biased P-body to N-Drift junction. The effect of using a buffer layer is shown in figure 6.7. If the buffer donor concentration, (where $N_d = d$) is optimised then the effect on ϵ_{MAX} will be negligible, therefore ($\epsilon_{MAX} = \epsilon_{MAX}'$) at a given level of V_{AK} . However, the electric field distribution becomes more trapezoidal than triangular, thus for a reduced base width (W_B') the PT-IGBT BV is identical to that of the NPT-IGBT, as demonstrated by the identical area under the electric field plot in figure 6.7.

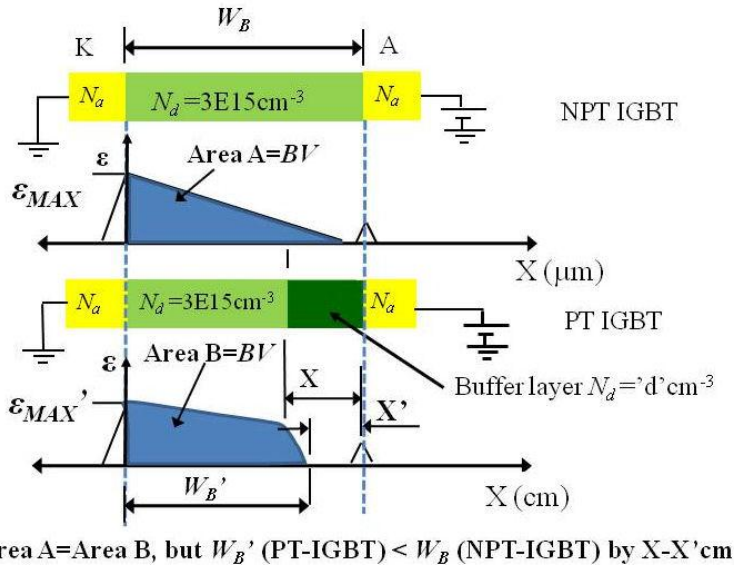


Figure 6.7. Effect of incorporating a buffer layer within an NPT IGBT to form a PT-IGBT using the field stop approach.

As mentioned earlier the extent of the depletion from the reversed biased junction of the P-body (collector of PNP BJT) into the N-Drift (base of the PNP BJT) may be restricted by use of a higher donor doping concentration in the base. Indeed graded impurity concentrations (highest at the emitter side of the base region) are used to increase the current gain of the PNP BJT by allowing conduction via drift in addition to diffusion as the concentration gradient sets up a small electric field across the base, as described by Grove[5] and Sze[3]. If the whole of the base region was uniformly increased then the BV of the

vertical VDMOSFET element would reduce greatly as shown by equation 6.1. The decision was therefore taken to trial the use of a buffer layer only in the N-Drift region of the lateral PiN diode, or base region of the lateral PNP BJT.

6.2.3 Optimised laterally injected hybrid

On this occasion the optimisation of the lateral buffer implant and field plate to obtain the best compromise of base width minimisation and blocking voltage was completed in a purely iterative manner as there were only two variables. The outcome of this iterative approach is the lateral hybrid structures as shown in figure 6.8. Figure 6.8 a) has an identical P-Anode (emitter) depth as was used in the simulated structures to this point while figure 6.8 b) has a P-Anode of reduced depth to $0.5\ \mu\text{m}$. Both these structures contained the identical gate length, cathode field plate length and N-buffer doping. A plot of the resultant doping concentration (both acceptors and donors) is shown in figure 6.9. The idea of using the stepped gradient for the buffer was taken from theory as presented by both Sze[3], and Grove[5] as to the use of a doping gradient in the base region of a BJT which was shown to decrease the transit time (t_{tr}) by adding an element of drift current to the otherwise diffusion current dependant base current transport, thus increasing the base transport factor (α_T). This however, would require a three mask ion implant which may not be acceptable in manufacture, Yoo[10].

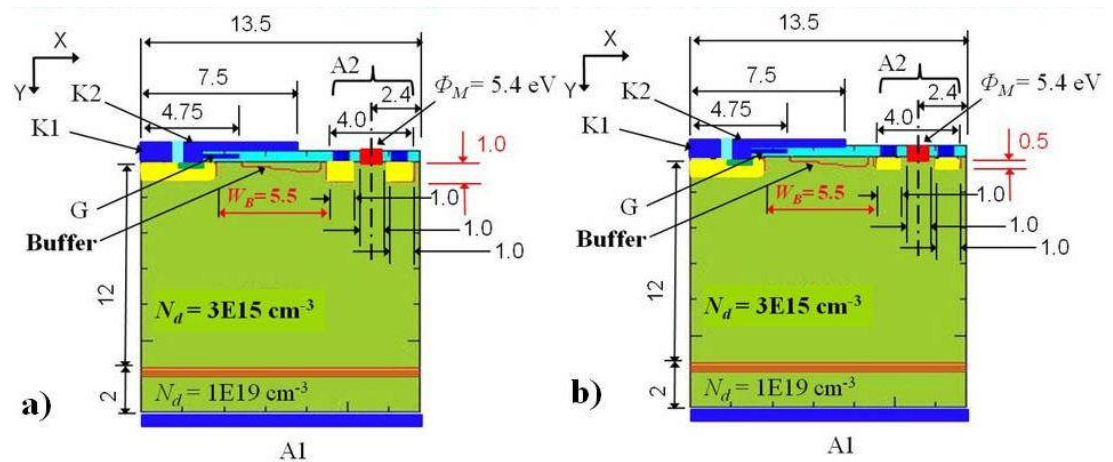


Figure 6.8. Structure of the optimised base width/BV laterally injected hybrid: a) with $1\ \mu\text{m}$ deep injectors and b) with $0.5\ \mu\text{m}$ deep injectors.

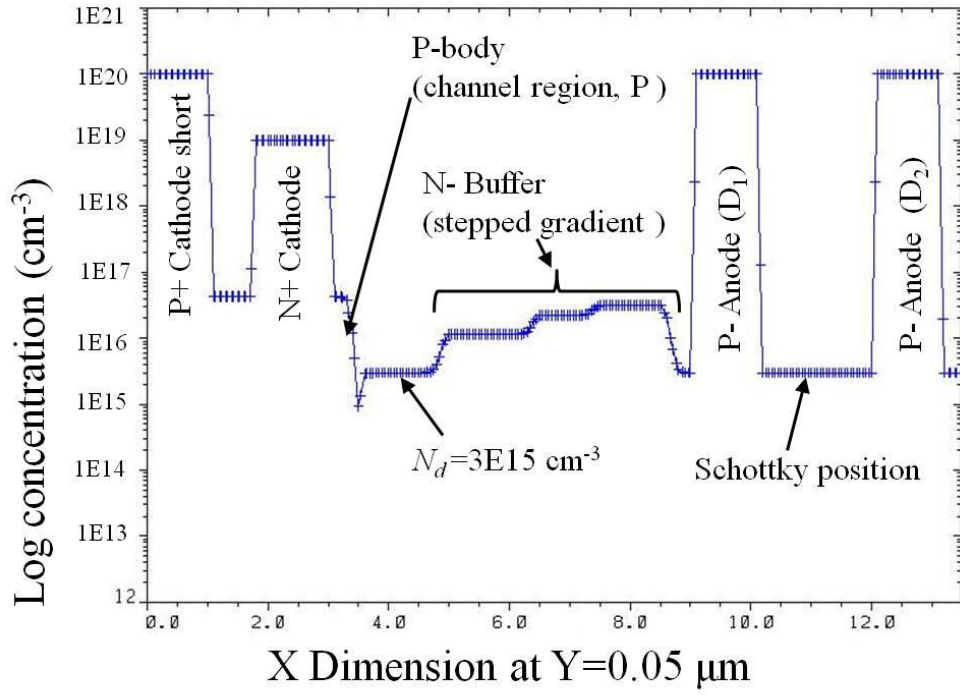


Figure 6.9. Impurity doping profile as used in the optimised hybrid structures of figure 6.8.

With $V_{GK} = 0$ V both of the structures shown in figure 6.8 were simulated to obtain the resultant blocking voltage (BV). The resultant electric field and avalanche current flow at the point of avalanche are shown in figures 6.10 and figure 6.11 respectively. The comparison of the I-V characteristics set against the 1-D or theoretical avalanche breakdown due to doping is shown in figure 6.12. As can be seen from figure 6.10 and 6.11 the buffer

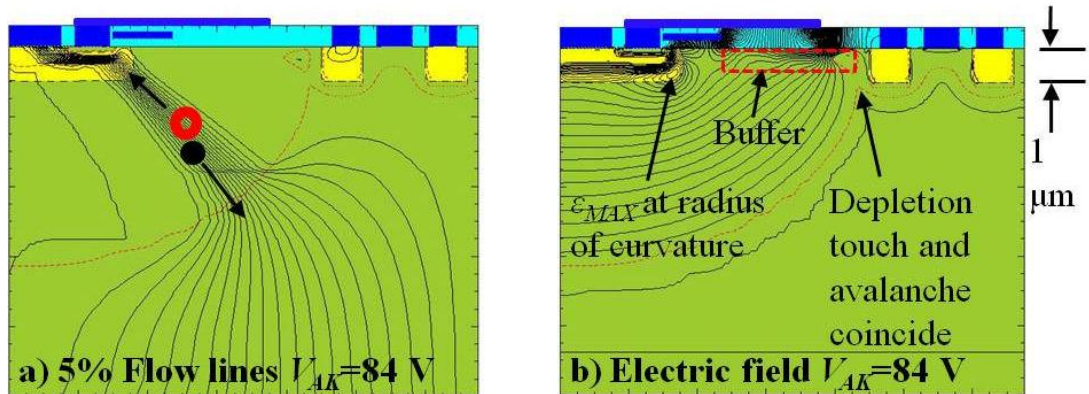


Figure 6.10. Two dimensional contour plots of: a) 5 % total current flow lines and b) electric field, for the structure shown in figure 6.8 a).

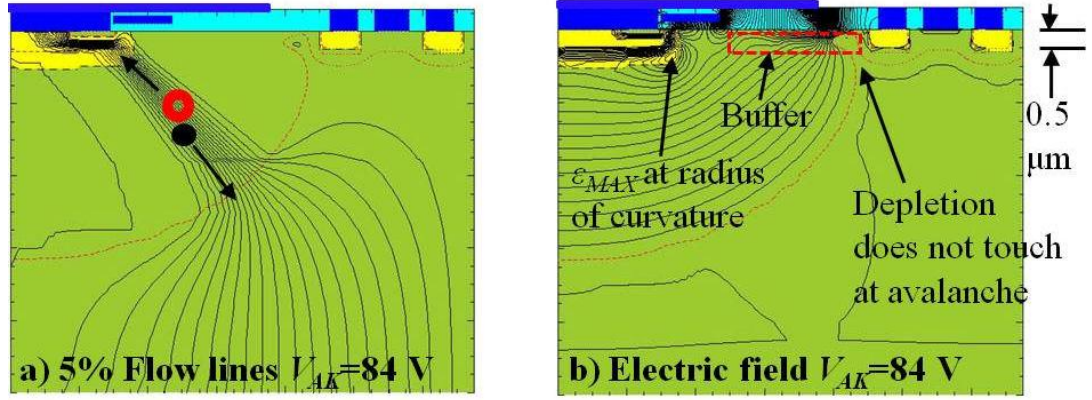


Figure 6.11. Two dimensional contour plots of: a) 5 % total current flow lines and b) electric field, for the structure shown in figure 6.8 b).

serves to impede the push out of the depletion extent from the reverse biased collector (P-body) into the N-Drift region (or base region). When the P-Anode was reduced in depth to $0.5 \mu\text{m}$ then the buffer implanted at a depth of $Y=0.25 \mu\text{m}$ prevented the punch through prior to avalanche conditions, thus punch through was prevented from causing further reduction of the blocking capability due to the exposed radius of curvature of the P-body. This was achieved in addition to the base width being reduced to only $W_B=5.5 \mu\text{m}$ hence providing improved PNP BJT performance in terms of t_{tr} , and α_T .

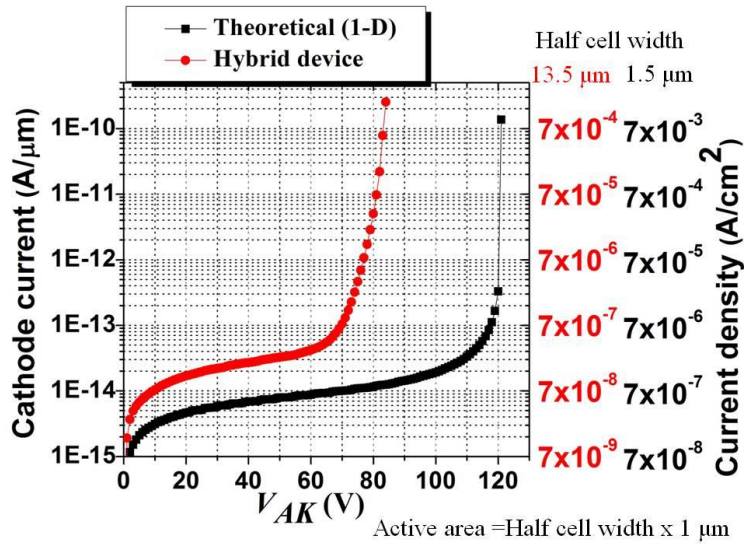


Figure 6.12. Direct comparison of blocking voltage for the structures shown in figure 6.8 (which coincide) and the theoretical (1-D) doping dependent blocking capability.

6.3 Comparison of vertical and lateral injected structures

Having now optimised the laterally injected structure for BV , V_{PT} and W_B a direct comparison could be made between with the vertical structure 1) of figure 5.11 in terms of their forward I-V characteristics and the achieved BV . The compared structures were as shown in figure 6.13, these were chosen because both these structures utilise a $12\ \mu\text{m}$ N-Drift layer thickness doped to $N_d = 3 \times 10^{15}\ \text{cm}^{-3}$, Schottky work function of $\Phi_M = 5.4\ \text{eV}$ and P-Anode acceptor doping (N_a) $= 1 \times 10^{19}\ \text{cm}^{-3}$. Each structure features the identical P-body design, but the base width (B_W) achieved in both structures is different and shown in red.

The resulting blocking voltage achieved by both the vertical and lateral structure as compared to the theoretical (1-D or doping dependent) result is shown in figure 6.14, noting that structure a) used the gate electrode as a field plate to shield the exposed P-body radius. Due to the use of the gate field plate to the full X dimension of the half cell, the vertical structure achieves a BV very close to the theoretical result. Whereas the lateral injected

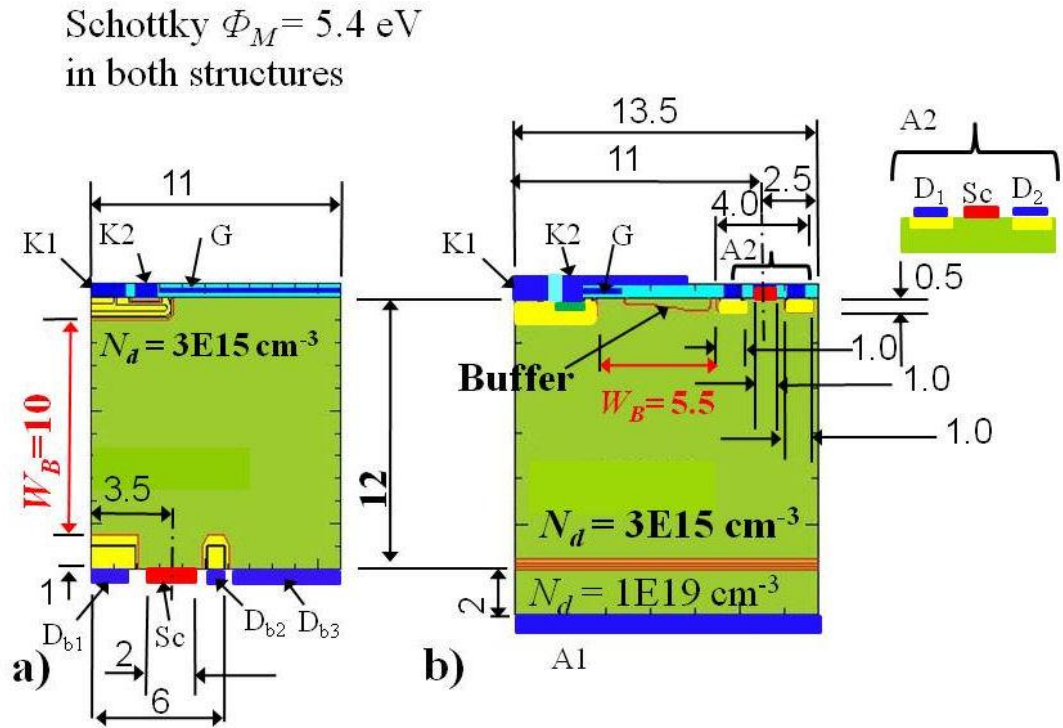


Figure 6.13. Compared structures a) vertical and b) lateral structures, each with $D_L = 12\ \mu\text{m}$ (where $N_d = 3 \times 10^{15}\ \text{cm}^{-3}$, P-Anode injector $N_a = 1 \times 10^{19}\ \text{cm}^{-3}$).

@ $V_{GK}=0$ V, V_{AK} = varied.

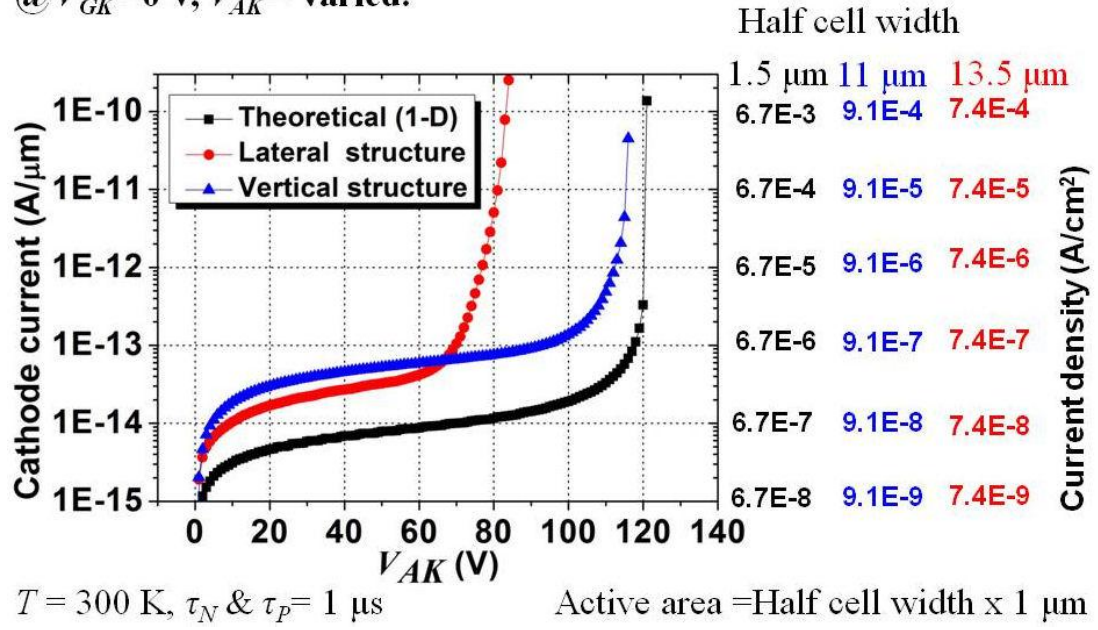


Figure 6.14. Comparison of blocking voltage achieved by the vertical and lateral hybrid structures as compared to the theoretical BV.

@ $V_{GK}=15$ V, V_{AK} = varied.

Active area = Half cell width \times 1 μm

$T = 300$ K, τ_N & $\tau_P = 1$ μs

Half cell width = 13.5 μm 11 μm

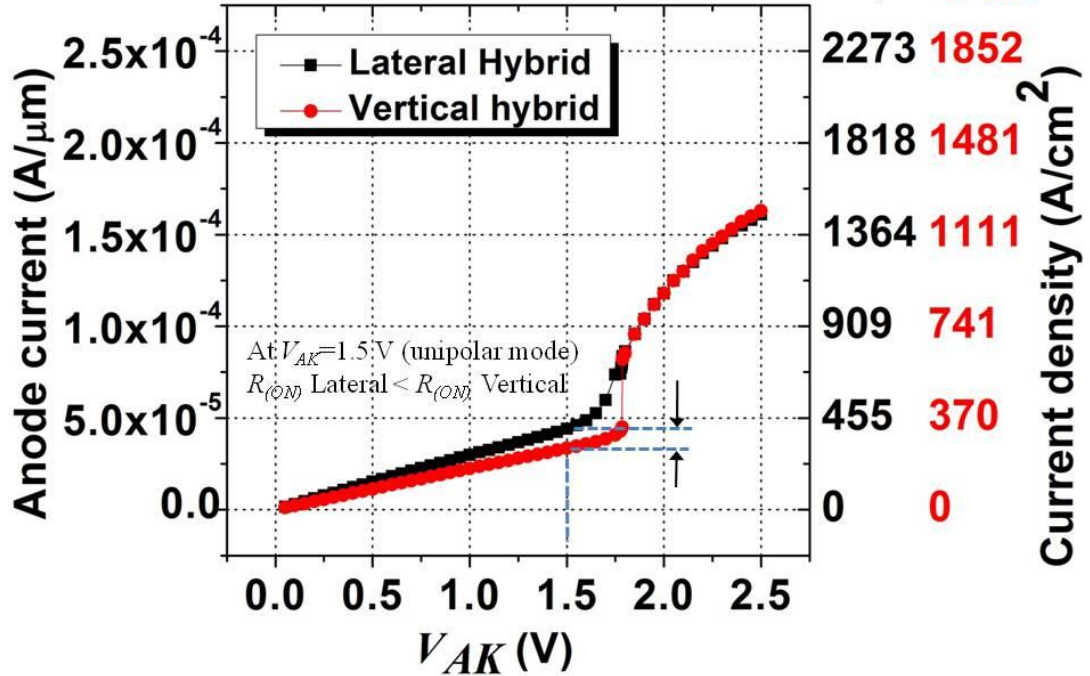


Figure 6.15. Comparison of forward I-V characteristics achieved by the vertical and lateral hybrid structures.

structure is adversely affected by the exposed radius of curvature. The comparison of forward I-V characteristics are shown in figure 6.15. The current density is shown as related to the half cell width of the structure. As regards the lateral structure then a comparison using the different current densities is not truly reflective as the half cell width of the lateral hybrid structure should also be to 11 μm as the P-Anode D₂, on the far right of figure 6.13 b), is not active in the PNP BJT due to the electron current from the MOS channel being taken by the P-Anode D₁ and the Schottky. Following the work of chapter 5 (figure 5.22) the lateral voltage (V_3+V_4) is equal to the vertical voltage (V_1). The unnecessary additional lateral length was required only to show the full injector as described in the JBS structures of chapter 4. However this was causing a possible reduction in the available lateral voltage developed within the half cell. Therefore it was hypothesised that a reduction of the half cell width would result in a higher voltage across $V_{EB} = V_3$, this would provide a reduced bipolar start up voltage and improved hole current flow.

From the results of figure 6.15 it would appear that the shorter base width (W_B) of the laterally injected hybrid did not provide a large benefit over the vertical structure in bipolar mode, an investigation of the level of V_{EB} (base to emitter voltage) achieved in each structure was therefore completed. The results shown in tables 6.1 and 6.2 were compiled

V_{AK} (V)	$V_3=V_{EB}$ (V)	K1 (I_C) (A/ μm)	K2(I_B) (A/ μm)	$D_{b1}+D_{b2} = I_E$ (A/ μm)
0.75	0.41	8.86E-13	1.69E-05	8.57E-13
1	0.53	3.06E-11	2.25E-05	2.91E-11
1.25	0.63	9.82E-10	2.80E-05	9.43E-10
1.5	0.73	2.90E-08	3.35E-05	2.82E-08
1.75	0.82	9.82E-07	4.07E-05	9.32E-07
2	0.89	3.45E-05	1.18E-04	-

Table 6.1. Voltage obtained at local bias point ($V_3=V_{EB}$) within vertical injected hybrid as a function of V_{AK} with $V_{GK}=15$ V.

V_{AK} (V)	$V_3=V_{EB}$ (V)	K1 (I_C) (A/ μ m)	K2(I_B) (A/ μ m)	$D_1+D_2 = I_E$ (A/ μ m)
0.75	0.33	1.52E-12	2.27E-05	2.14E-12
1	0.44	9.37E-11	2.99E-05	9.56E-11
1.25	0.54	5.45E-09	3.67E-05	5.47E-09
1.5	0.64	2.35E-07	4.38E-05	2.35E-07
1.75	0.74	8.86E-06	6.48E-05	8.40E-06
2	0.77	2.62E-05	9.22E-05	2.40E-05

Table 6.2. Voltage obtained at local bias point ($V_3=V_{EB}$) within lateral injected hybrid as a function of V_{AK} with $V_{GK}=15$ V.

using the QFN results at $X=3.5, 5.5$ and $8 \mu\text{m}$ as shown in figure 5.15 & 5.16 from chapter 5 (and at other bias voltages) for the vertical structure. These were compared to the QFN results at $Y=0.05 \mu\text{m}$ using the same method as shown in figure 5.31, for the lateral structure of figure 6.13 b.

A comparison of the resultant semi-log current versus V_{EB} plots for both the vertical and laterally injected hybrids are shown in figures 6.16 and figure 6.17 respectively. Although the resultant collector currents are almost equal at $V_{AK}=2$ V, due to the larger recombination in the wider base region of the vertically injected hybrid) these plots graphically confirm the effects of the low V_{EB} bias achieved in the laterally injected structure. The slight increase in I_C over I_E at $V_{EB} = 0.77$ V, as shown in figure 6.17, within the laterally injected structure was due to hole storage in the base region from forward conduction of the Schottky contact which caused a slight increase in the open base gain (α) of the lateral device.

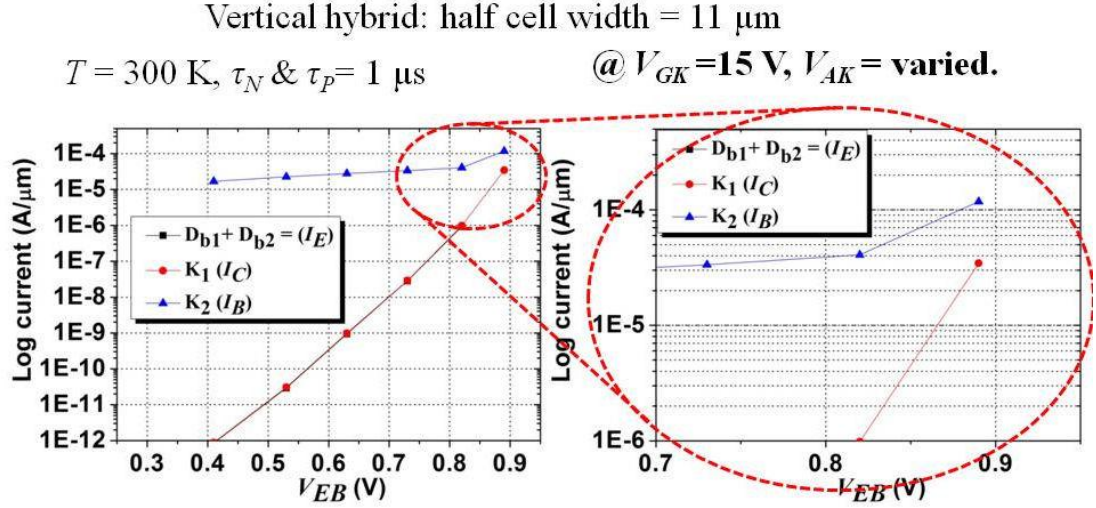


Figure 6.16. Semi log plot of current versus V_{EB} for vertical injected hybrid (half cell width = 11 μm).

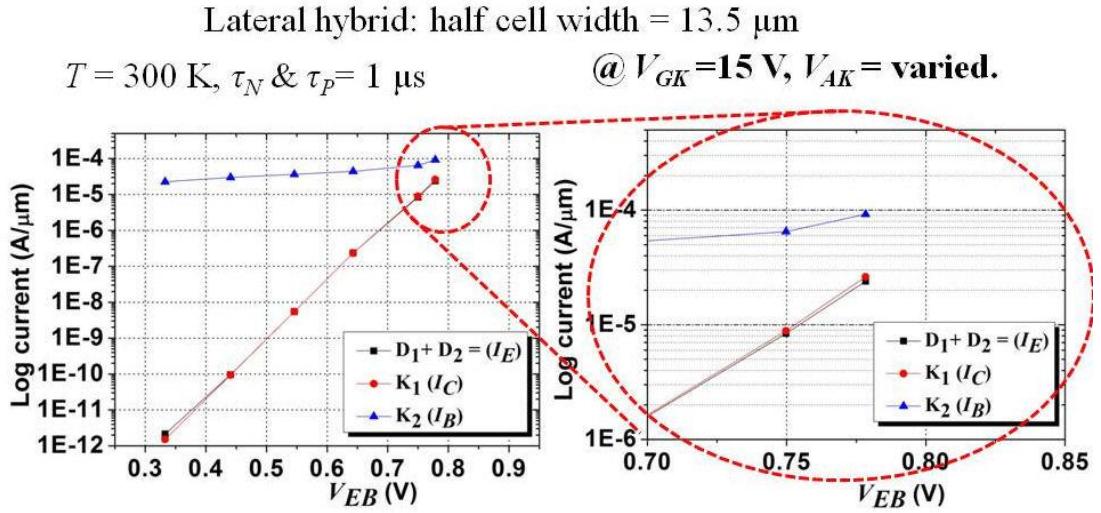


Figure 6.17. Semi log plot of current versus V_{EB} for lateral injected hybrid (half cell width = 13.5 μm).

6.4. Increasing V_{EB} as achieved within lateral structure

The Kirchhoff equivalent circuit of the hybrid in unipolar mode from chapter 5 is repeated in figure 6.18. Figure 6.18 indicates the nodal electron current flow and the voltages developed across each of the elements, noting that the voltages V_4 and V_3 are developed within the lateral PiN diode structure between the P-Anode of D_1 and the N^+ cathode via the inverted channel.

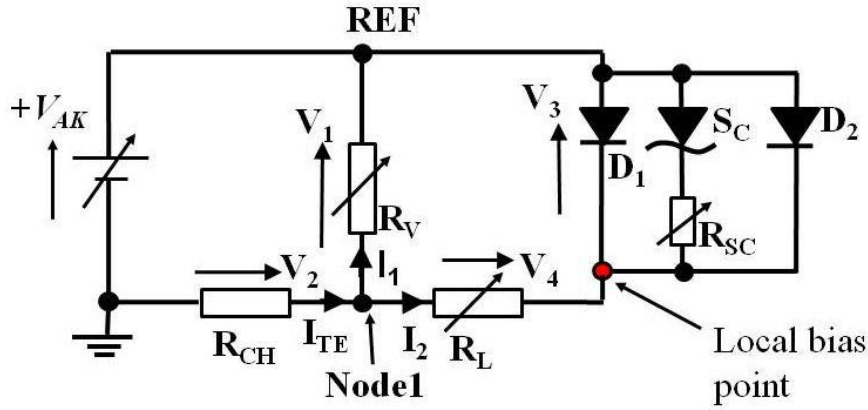


Figure 6.18. Kirchhoff equivalent circuit of the hybrid structure in unipolar mode.

From figure 6.18 it is clear to see that, as discussed in chapter 5, $V_1 = V_3 + V_4$ in unipolar mode. In bipolar mode the equivalent circuit is as shown in figure 6.19. Again, the emitter to base voltage V_{EB} continues to $= V_3 = V_{SC}$, as formed across the Schottky contact. The voltage V_4 becomes effectively the PNP base resistance of the neutral region (W_{B-EFF}). However, due to conductivity modulation within the base then V_4 becomes reduced when the PNP BJT is activated. The voltage drop across the reverse biased collector – base junction, associated with the depletion region, is indicated in figure 6.19 as V_5 , in addition a resistor has been included ($R_{collector}$) to indicate the resistance of the hole current path to ground through the P-body which is entirely doping dependent (where peak $N_a = 1.15E-17 \text{ cm}^{-3}$).

As can be seen from both figures 6.18 and 6.19 the voltage formed across the vertical N-Drift length (V_1) not only has a direct effect on the voltages V_3 and V_4 in unipolar mode, but this continues in bipolar mode. The difference is that in bipolar mode as discussed in chapter 5 the high work function Schottky has begun to conduct subsequent to conductivity modulation (at around $V_{AK} = 1.5 \text{ V}$). After the Schottky conducts then V_1 , $V_3 + V_4$ and V_{SC} must be equal and so the electron currents I_1 , I_2 and I_3 adjust accordingly. The Schottky therefore acts as a ‘safety valve’ to reduce current I_2 , the electron current into the emitter ($I_{diff,E}$), thus reducing the injected hole supply and therefore preventing $V_{EB} = V_3$ rising with the hole concentration in the base (as per the use of a solid P-Anode structure

without Schottky as demonstrated in chapter 5). The hole supply would therefore be constrained by the Schottky action.

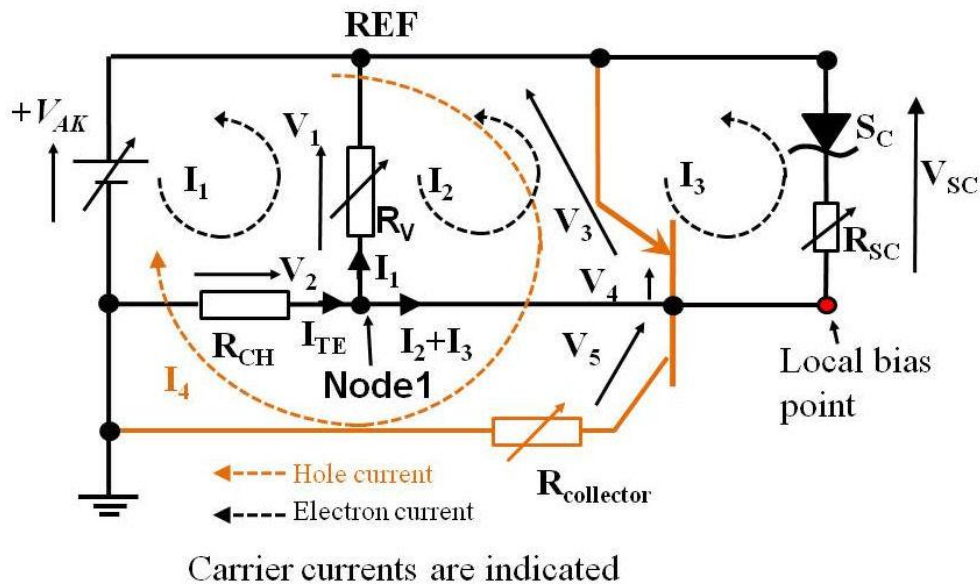


Figure 6.19. Equivalent circuit of the hybrid in bipolar mode.

Following the work of chapter 5 it became apparent from the equivalent circuits provided that two possible methods were available to increase the V_{EB} voltage within the lateral structure:-

- Decrease the simulated half cell width of the lateral structure
- Increase the vertical drift length of the lateral structure

The effects of both these were investigated on the resultant I-V characteristics and V_{EB} .

6.4.1 Effect of decreasing half cell width in the lateral hybrid

The structures investigated are shown in figure 6.20. The original lateral structure as was shown in figure 6.8 b) is repeated in figure 6.20 b), this was to be compared with the identical structure, but on this occasion the half cell was reduced to reflect the true half cell for the hybrid at a half cell width of 11 μm as shown in figure 6.20 a).

The resultant I-V characteristics of the reduced half cell width structure are shown in figure 6.21. In this figure a comparison is made to the optimised VDMOSFET (but with modified half cell width to 11 μm wide), the lateral hybrid with a 13.5 μm half cell and the

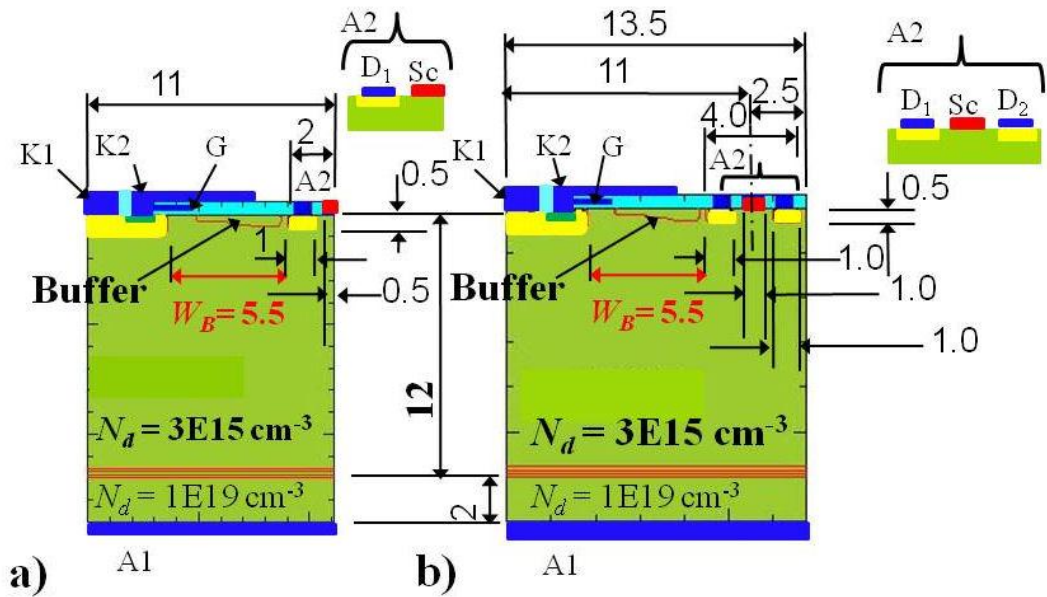
Schottky $\Phi_M = 5.4$ eV, P-Anode $N_a = 1 \times 10^{19} \text{ cm}^{-3}$ in both structures

Figure 6.20. Compared lateral structures showing reduced half cell width to a) 11 μm from b) 13.5 μm .

vertical hybrid structure of figure 6.13 a). Immediately from this plot the reduced half cell width lateral structure, of 11 μm wide, can be seen to demonstrate a reduced bipolar turn on voltage (V_i). In this case a reduction of 0.25 V as compared to the 13.5 μm wide lateral hybrid is achieved. This is due to a larger V_{EB} being developed within the shorter cell width structure as shown in figure 6.22. The resultant V_{EB} , as demonstrated in chapter 5, is dependent upon the hole concentration in the base (see equation 5.8).

As the concentration in the vertical structure is a result of lateral resistive biasing along the P-Anode the V_{EB} the bias achieved is higher in that structure than in the lateral structures, which are dependent upon minority carrier diffusion into the base, or N-Drift region of the lateral PiN diode. Despite the higher V_{EB} developed in the vertical hybrid unfortunately, the larger base width means that fewer of the resultant holes reach the collector due to recombination in the base, Grove [5]. In comparison the shorter base width within the lateral structure of figure 6.20 a) has a lower achieved level of V_{EB} at any given V_{AK} , and yet obtains a higher collector current as shown by comparison of the semi-log plots

of current against V_{EB} in figures 6.23 and 6.16. Indeed comparison of figures 6.23 and 6.17 indicate that the collector current of the 11 μm half cell as compared to the other lateral

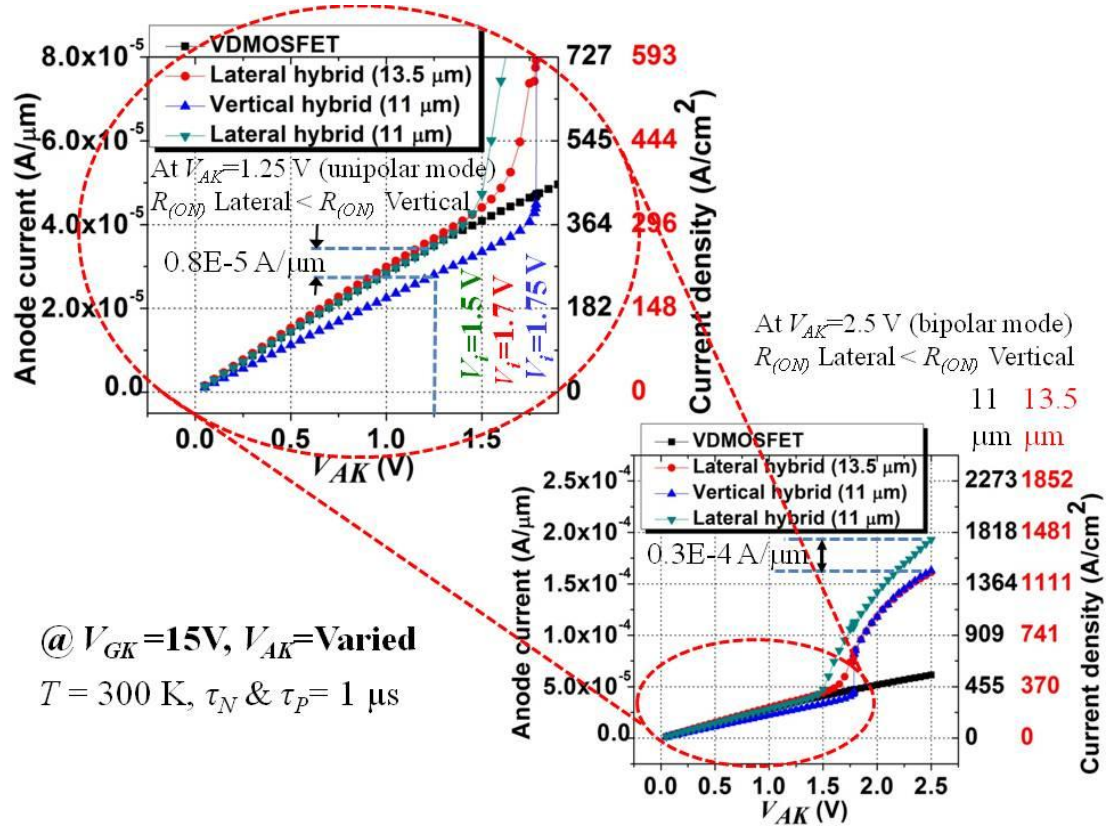


Figure 6.21. Comparison of I-V characteristics of the lateral and vertical hybrids compared to the optimised VDMOSFET of 11 μm wide half cell.

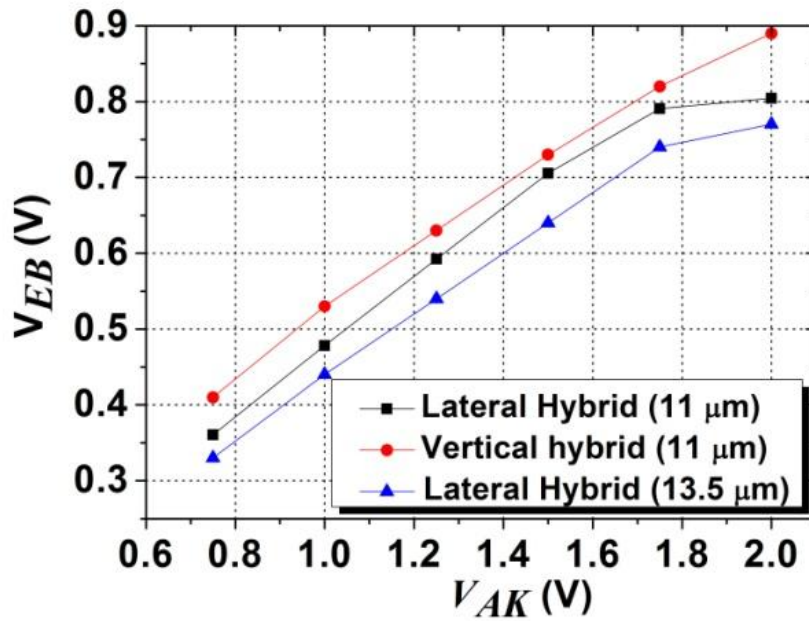


Figure 6.22. Comparative plot of achieved V_{EB} versus V_{AK} terminal bias for various hybrid structures.

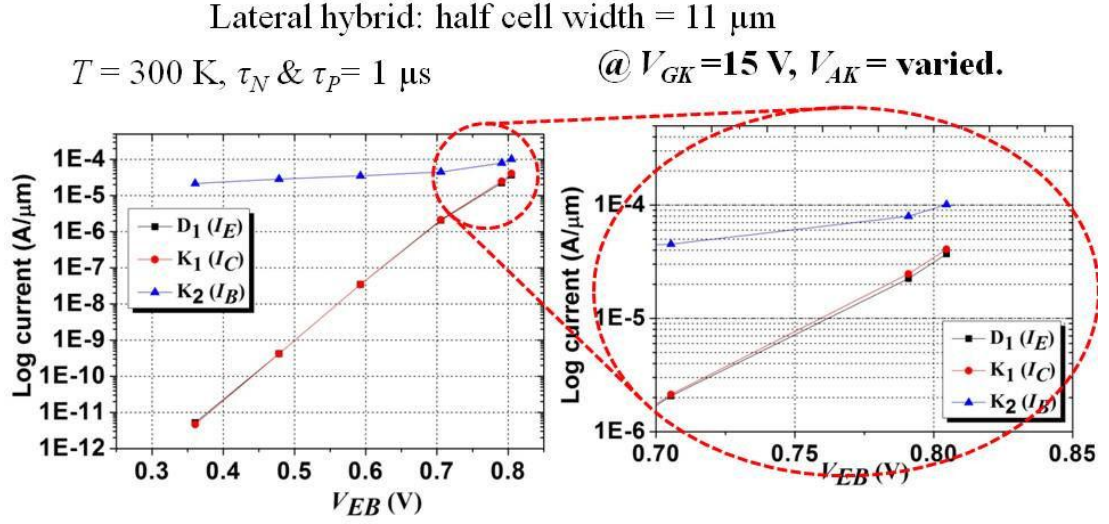


Figure 6.23. Semi log plot of the lateral hybrid structure of 11 μm wide half cell.

structure of 13.5 μm half cell also showed a marked increase due purely to the difference in V_{EB} . The V_{EB} in the lateral structures is hindered from rising further by the conduction of the Schottky, the Schottky does not otherwise affect performance. Whereas in the vertical structure V_{EB} is allowed to rise in line with the hole concentration in the base because the conduction of the Schottky acts only to reduce the saturation current level and the bipolar start up voltage, which is determined by Φ_M , as shown in figure 5.17.

6.4.2 Effect of increasing vertical drift length in the lateral hybrid

The three structures analysed are shown in figure 6.24. These structures were identical to that shown in figure 6.20 b) except that the drift length was varied in the range 12 \pm 2 μm and the P-Anode (emitter) was doped to $N_a = 1 \times 10^{20} \text{ cm}^{-3}$ to ensure depletion of the P-Anode would be delayed in terms of V_{AK} . The method again was to obtain the quasi Fermi potential for electrons at $Y = 0.05 \mu\text{m}$ as demonstrated in chapter 5 (figure 5.31) and use that data to ascertain the value of V_{EB} for the various lateral hybrid structures. Using the obtained data the semi-log plot of I_B and I_C versus V_{EB} can be constructed using the I-V characteristics

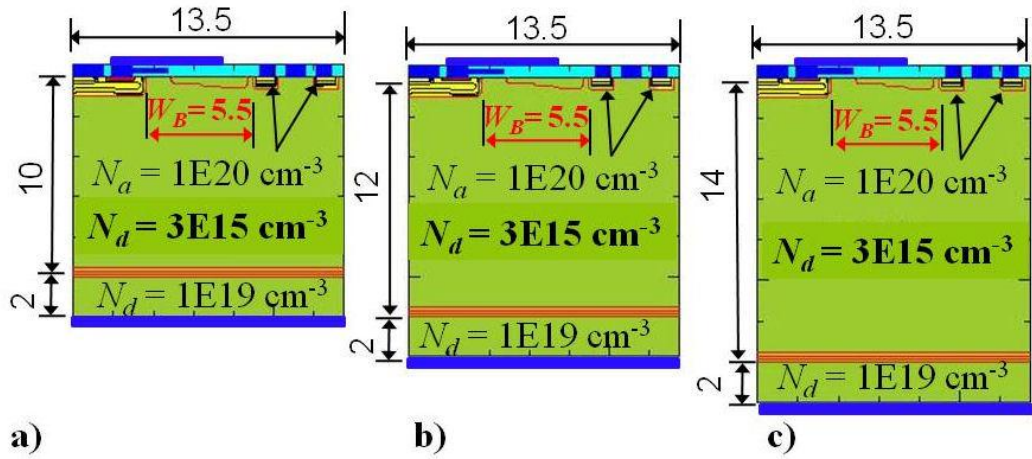


Figure 6.24. Structures of differing drift length as used to assess the effect on the PNP BJT performance.

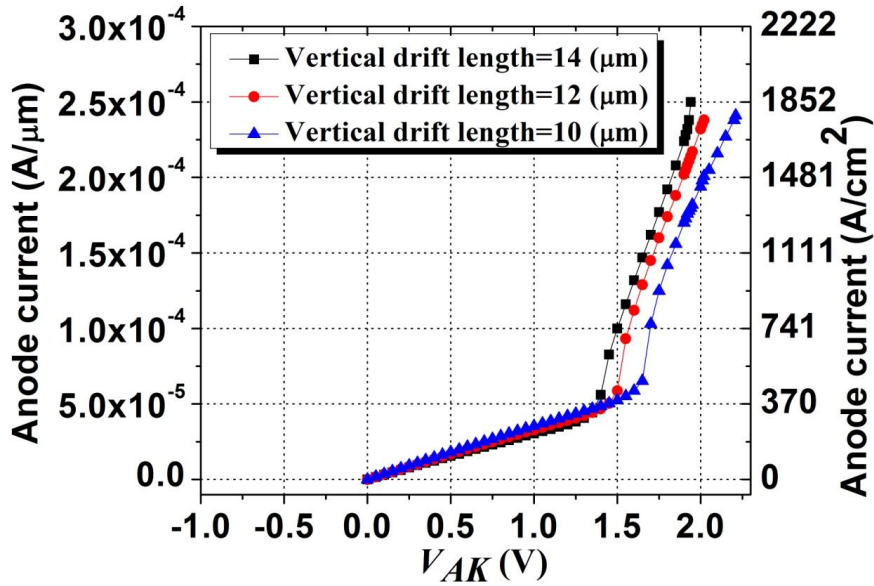


Figure 6.25. Forward I-V characteristics of three compared lateral hybrid structures from figure 6.24 at $V_{GK}=20$ V.

data obtained at $V_{GK}=20$ V. The comparison of the resultant I-V characteristics for each of the structures depicted within figure 6.24 is shown in figure 6.25. The effect of the vertical drift length on V_{EB} is shown in figure 6.26. As can be seen in the I-V characteristics of figure 6.25 as expected the reduction in drift length had the effect of reducing the $R_{(ON,SP)}$ of the unipolar part of the characteristic, Baliga [1]. However, from figure 6.26 the effect of reducing the drift length was to decrease V_{EB} , hence a compromise existed within the lateral hybrid between the unipolar performance (in terms of $R_{(ON,SP)}$) and the bipolar performance

of the PNP BJT, in terms of collector current magnitude for a given terminal voltage (V_{AK}) as limited by the V_{EB} achieved within the structure at that bias voltage.

A comparative plot of the current and voltage dependencies within a lateral hybrid with drift region of 12 μm is shown in figure 6.27, and tables 6.3 to 6.6 show the relevant data for each drift length variant. After the bipolar mode is entered within the lateral

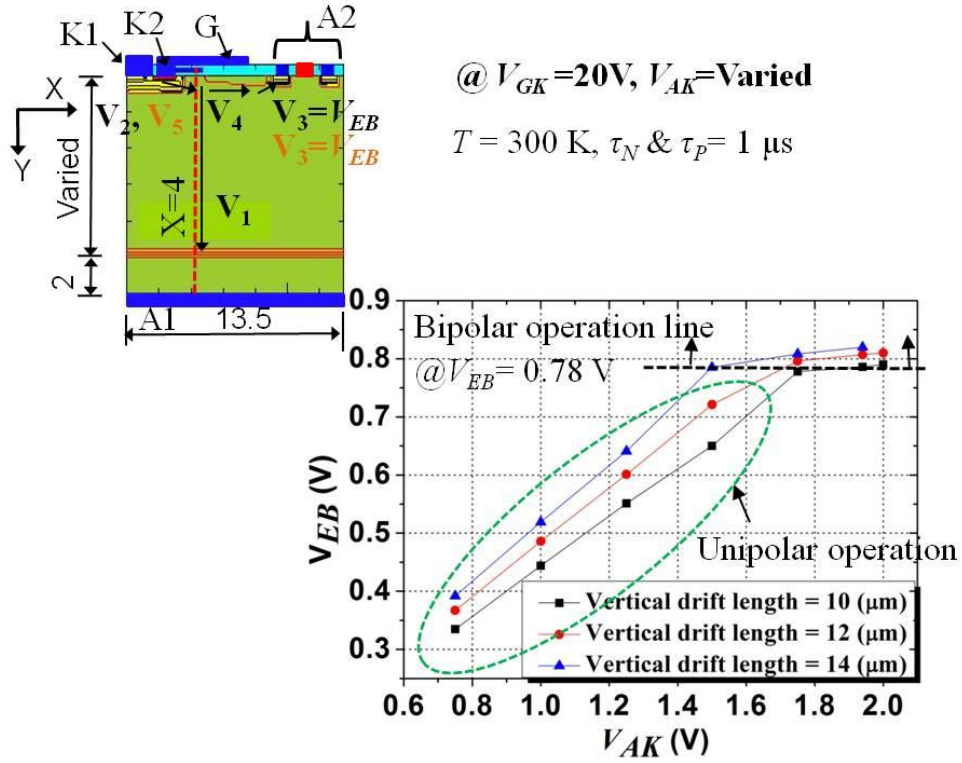


Figure 6.26. Plot of V_{EB} versus V_{AK} for structures of varied vertical drift length.

hybrid, the Schottky (Sc), as indicated in the equivalent circuit of figures 6.26 and 6.27, begins to conduct (at $V_{AK} = 1.5$ V). This low resistance conductance path reduces the current flow ($I_2 = I_{diff,E}$) available to the emitter, thus the rate of V_{EB} reduces in line with the hole concentration in the base, hence the Schottky effectively ‘clamps’ the V_{EB} level achieved as shown in figure 6.26. Thereafter the V_{EB} level rises only slowly, until it reaches a peak which remains relatively constant as dictated by the drift voltage $V_1 = V_3 + V_4$ where $V_{EB} = V_3$. Whereas the voltage V_3 is fixed by the hole concentration in the base (equation 5.8), as a consequence of entering bipolar mode V_4 and V_1 must reduce proportionally due to conductivity modulation effects to ensure the equality remains true. As stated the hole

concentration in the base, is limited by the Schottky conduction, and the voltage V_1 is proportional to the extent of the conductivity modulated region, noting that the largest volt drop will occur in the non conductivity modulated part of that vertical drift region. Once the conductivity modulated region extends to the N+ substrate then the voltage V_1 has reached its minima and can reduce no more, thereafter only the variation in current (I_1) will adjust voltage V_1 . This is the point at which V_4 and V_1 stabilise and V_{EB} peak is reached. Once the hole concentration in the base has been limited by the bounds of the voltage/current dependencies then V_{EB} can increase no more.

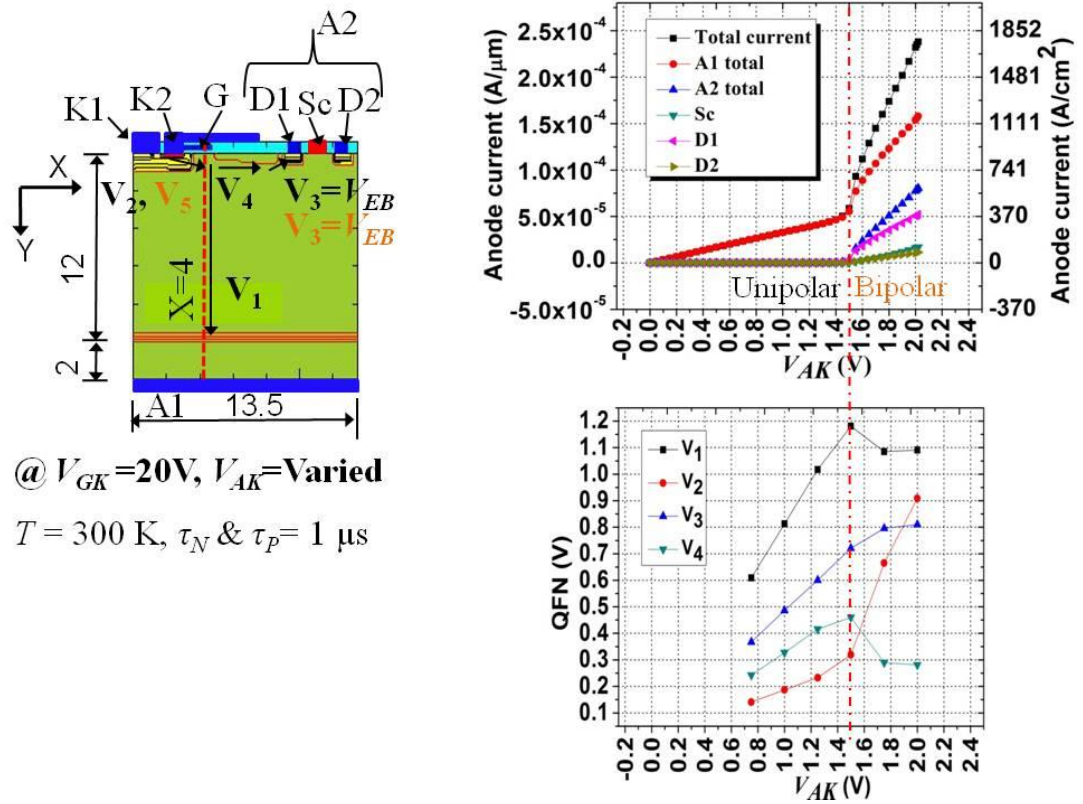


Figure 6.27. Comparative plot of the terminal currents and internal voltages developed within the lateral hybrid with 12 μm epitaxial layer thickness.

For the 12 μm example, as shown in figure 6.27, then immediately upon entry into bipolar mode at $V_{AK} = 1.5$ V, any further increase in V_{AK} appears across the reverse biased collector to base junction (V_5), hence the voltage V_2 (red trace) immediately begins to rise. V_2 is the voltage drop across the channel in unipolar mode, but as shown in figure 6.19 in bipolar mode V_2 operates in parallel with V_5 , the reverse biased collector to base junction. V_2 is therefore increased in line with V_5 (as shown in the figures in blue in the V_2 columns of

tables 6.3 to 6.6). In proportion to this increased voltage drop the collector to base electric field and hence charge increases, but the collector to base depletion extent remains static due to the increased carrier concentration in the base. Thus, the effective base width (W_{B-EFF}) also remains approximately static. The effect known as the Early effect (Early[11]) therefore only occurs in a limited way at these low voltage levels ($V_{AK}=1-2V$), but further increases in V_{AK} bias would bring about a reduced effective base width and hence increased hole current at the collector.

V_{AK} (V)	V @ $X=4$ (V)	V@ $X=9$ (V)	V_1 (V)	V_2 (V)	$V_3=V_{EB}$ (V)	$V_4=V_N$ (V)	$K_1(I_C)$ (A/ μ m)	$K_2(I_B)$ (A/ μ m)	D_1+D_2 (I_E) (A/ μ m)
0.75	0.152	0.415	0.598	0.152	0.335	0.263	1.51E-12	2.69E-05	2.31E-12
1	0.202	0.556	0.798	0.202	0.444	0.354	9.92E-11	3.54E-05	1.02E-10
1.25	0.25	0.699	1	0.25	0.551	0.449	6.30E-09	4.36E-05	6.32E-09
1.5	0.304	0.85	1.196	0.304	0.65	0.546	2.93E-07	5.22E-05	2.94E-07
1.75	0.591	0.972	1.159	0.591	0.778	0.381	2.31E-05	1.02E-04	2.15E-05
2	0.864	1.21	1.136	0.864	0.79	0.346	4.78E-05	1.46E-04	4.36E-05

Table 6.3. Results for structure with 10 μ m epitaxial layer thickness

V_{AK} (V)	V @ $X=4$ (V)	V@ $X=9$ (V)	V_1 (V)	V_2 (V)	$V_3=V_{EB}$ (V)	$V_4=V_N$ (V)	$K_1(I_C)$ (A/ μ m)	$K_2(I_B)$ (A/ μ m)	D_1+D_2 (I_E) (A/ μ m)
0.75	0.141	0.383	0.609	0.141	0.367	0.242	5.25E-12	2.49E-05	6.25E-12
1	0.187	0.514	0.813	0.187	0.486	0.327	5.05E-10	3.28E-05	5.09E-10
1.25	0.233	0.649	1.017	0.233	0.601	0.416	4.40E-08	4.06E-05	4.41E-08
1.5	0.319	0.779	1.181	0.319	0.721	0.46	3.43E-06	5.53E-05	1.46E-05
1.75	0.665	0.954	1.085	0.665	0.796	0.289	4.10E-05	1.19E-04	3.72E-05
2	0.909	1.19	1.091	0.909	0.81	0.281	6.83E-05	1.63E-04	6.15E-05

Table 6.4. Results for structure with 12 μ m epitaxial layer thickness

V_{AK} (V)	V @ $X=4$ (V)	V @ $X=9$ (V)	V_1 (V)	V_2 (V)	$V_3=V_{EB}$ (V)	$V_4=V_N$ (V)	$K_1(I_C)$ (A/ μ m)	$K_2(I_B)$ (A/ μ m)	D_1+D_2 (I_E) (A/ μ m)
0.75	0.133	0.358	0.617	0.133	0.392	0.225	1.43E-11	2.31E-05	1.55E-11
1	0.177	0.481	0.823	0.177	0.519	0.304	1.87E-09	3.04E-05	1.87E-09
1.25	0.223	0.609	1.027	0.223	0.641	0.386	1.99E-07	3.81E-05	1.99E-07
1.5	0.446	0.715	1.054	0.446	0.785	0.269	2.19E-05	7.82E-05	2.00E-05
1.75	0.694	0.942	1.056	0.694	0.808	0.248	5.30E-05	1.24E-04	4.76E-05
1.94	0.875	1.12	1.065	0.875	0.82	0.245	8.13E-05	1.69E-04	7.29E-05

Table 6.5. Results for structure with 14 μ m epitaxial layer thickness

The slight increase in $V_{EB} = V_3$ after $V_{AK}=1.5$ V is due to the slight increase in hole concentration following entry into bipolar conduction mode until the above described concentration limit is reached as dictated by the voltage – current dependencies for each given drift length variant.

The resultant magnitude of V_{EB} is clearly increased with increase in vertical drift length, as shown in figure 6.26, and this is maintained in bipolar mode, with each drift region variant finding its own internal current/voltage balance. As a direct result of the magnitude of V_{EB} developed across the base to emitter junction the performance of the PNP BJT in each vertical drift length variant can be plotted. The semi log plots of base current (I_B), emitter current (I_E) and collector current (I_C) against V_{EB} are shown in figures 6.28 a through to c. The emitter current used in this case is the sum of the currents via P-Anodes D_1 and D_2 .

As can be seen from figure 6.28, the first point to note is that common emitter gain ($\beta = I_C/I_B$) is less than 1 (as indicated by the vertical separation between I_B and I_C , at any given value of V_{EB}). The fact that the base current is higher than the collector current is not

surprising as the base current as supplied via the inverted MOS channel which also supplies the drain of the VDMOSFET or anode 1 of the hybrid. The common emitter gain (β) however increases with increased vertical drift length due to the associated increase in V_{EB} . Secondly, the common base gain (α) is also equal to 1 (as indicated by the vertical separation between I_C and I_E , at any given value of V_{EB}). However, using the example I-V characteristics for the structure with a 12 μm vertical drift length, as shown in figure 6.27, and comparing that to figure 6.28 b) then a slight common base gain improvement occurs

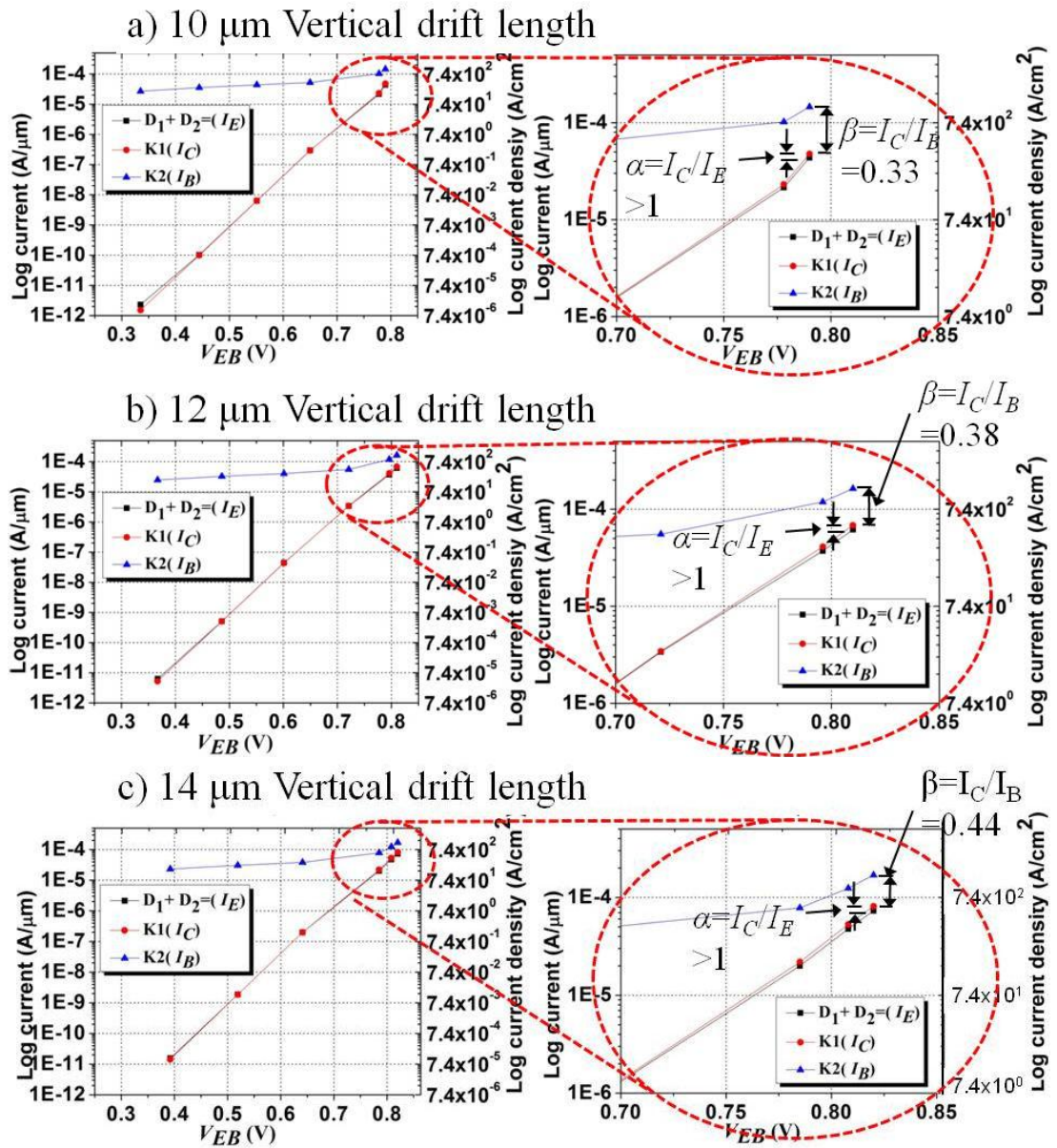


Figure 6.28. Semi-log plot of the PNP BJT currents versus V_{EB} for varying vertical drift length.

after the Schottky begins to conduct at $V_{AK}=1.5$ V due to the storage of holes in the drift region in accordance with the work of Scharfetter[12] and Jager[13], thereafter ($\alpha > 1$).

The common emitter current gain (β) is low in all cases (figure 6.28 a through c) due to the higher donor concentration in the base region subsequent to the onset of conductivity modulation as described by Baliga[1]. The increased donor concentration in the base enhances the injection of electrons into the P-Anode (emitter) which reduces the emitter efficiency (γ) and hence results in a low β known as the Webster's effect, Webster[14]. It is important to note that the main benefit of increasing the vertical drift length is to improve the magnitude of hole current ($I_{diff,B}$) flowing to the collector. This can be seen by comparison of the collector current magnitude achieved within the various structures as shown in figures 6.28 a through to c. The best PNP BJT contribution is achieved in the structure with the longest vertical drift region and hence highest $R_{(ON,SP)}$ in unipolar mode. Thus, a compromise must be sought for the lateral hybrid which would depend on the requirements of any given switching application.

6.5 Summary

In this chapter the laterally injected hybrid was optimised in order to obtain the best compromise of PNP performance (in terms of β and α) and BV . This requires reduced base width (W_B) whilst avoiding V_{PT} , but maximising BV requires increased W_B . If a Non Punch Through IGBT was to be used then the minimum base width was calculated at $6.62 \mu\text{m}$ when using a base region donor concentration of $N_d=3\text{E}15 \text{ cm}^{-3}$ to achieve $BV=100$ V. In order to achieve the lowest injection start up voltage (V_i), W_B had to be minimised below $6.62 \mu\text{m}$, but at the risk of reducing V_{PT} .

The optimum setting of W_B at $5.5 \mu\text{m}$ was achieved in the lateral hybrid by use of a lateral N-buffer to form a lateral Punch through (PT) type IGBT. This structure enabled a reduction in W_B to $5.5 \mu\text{m}$, thus improving the PNP BJT performance while ensuring that $V_{PT} > BV$.

The $R_{(ON,SP)}$ to BV comparison plot of the lateral and vertical hybrid is shown in figure 6.29. These are of the identical half cell width ($11\ \mu\text{m}$), vertical drift length (D_L), N-Drift doping ($N_d=3\text{E}15\ \text{cm}^{-3}$), P-Anode doping ($N_a=1\text{E}19\ \text{cm}^{-3}$) both at a gate voltage ($V_{GK}=15\ \text{V}$). A comparison summary of using the novel merged Schottky injector within the vertical and lateral hybrid structures is shown in table 6.6.

When the optimised lateral structure was compared directly to the vertical hybrid structure the achieved BV was lower ($84\ \text{V}$ to $116\ \text{V}$ respectively) as shown in figure 6.29.

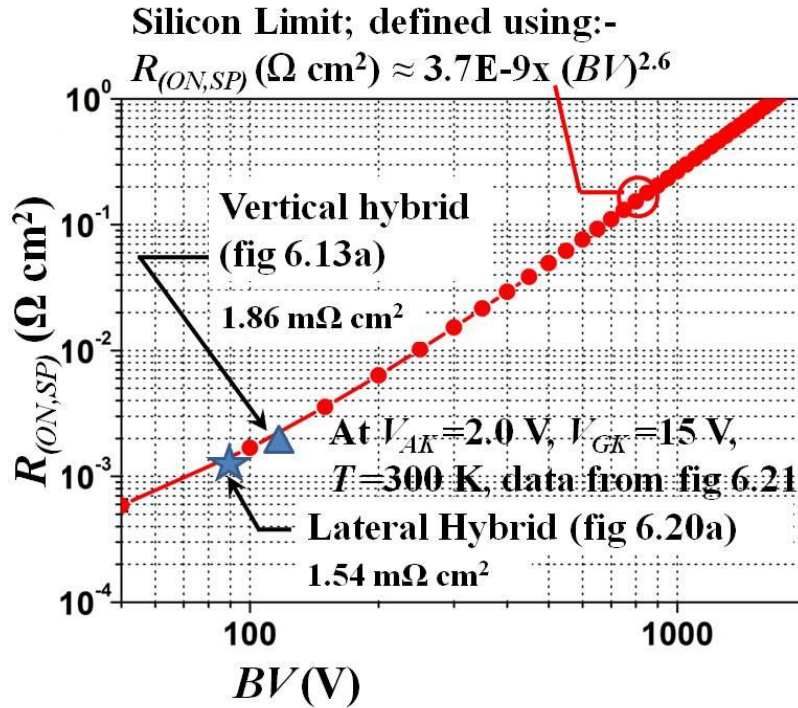


Figure 6.29. Comparison of $R_{(ON,SP)}$ vs BV for lateral and vertical hybrid structures.

The reduced BV of the lateral hybrid was due to the reduction in the open base transistor breakdown voltage (BV_{CEO}) of the PNP structure with reduced $W_B=5.5\ \mu\text{m}$, whereas in the vertical structure $W_B=10\ \mu\text{m}$. The base to emitter bias (V_{EB}) achieved in the vertical hybrid was found to be higher than in the lateral structure of the same cell width and vertical drift length and with the same merged Schottky anode design. Though the lower base width of the lateral structure meant that PNP performance was comparable, indeed the $R_{(ON,SP)}$ at $V_{GK}=15\ \text{V}$ coincided with the calculated 1-D silicon limit line with both structures. Therefore

there was no discernible difference in performance at $V_{AK} = 2$ V (bipolar mode), $V_{GK} = 15$ V. Due to the reduced V_i of the lateral hybrid however, as shown in figure 6.21, it was concluded that with increased gate bias the lateral structure would offer an increased reduction in $R_{(ON,SP)}$ than the vertical structure below the silicon limit line. Using I-V data from figure 6.25 then the lateral hybrid with 12 μm vertical drift length at $V_{GK} = 20$ V, $V_{AK} = 2$ V achieved an $R_{(ON,SP)}$ of $0.916 \text{ m}\Omega\text{cm}^2$. In addition the lateral hybrid achieved a lower $R_{(ON,SP)}$ in unipolar mode as shown in figure 6.21 as no vertically placed P-Anode impeded the electron current to the bottom anode (A1). Importantly, the half cell width of the vertical structure could not be reduced further without the $R_{(ON)}$ of the electron current in unipolar mode increasing, which was undesirable as it was detrimental to the aim to provide lowest static loss in both unipolar and bipolar mode. If the P-Anode length in the vertical hybrid was reduced from 6 μm to 3.5 μm to enable a reduction unipolar mode $R_{(ON)}$ then from the work of chapter 5 (figure 5.10) then the bipolar start up voltage would increase to $V_i = 2.75$ V which would be detrimental to the static loss in bipolar mode.

Within the lateral structure, a method was proven to increase the V_{EB} bias hence improving the emitter injection efficiency (γ) and the magnitude of the collected hole current. This method was to increase the vertical drift length which, albeit slightly detrimental to the unipolar mode $R_{(ON)}$, resulted in the laterally injected hybrid achieving a decreased bipolar start up voltage (V_i) and improved PNP BJT performance under the same bias conditions, due to the increased V_{EB} at any given level of V_{AK} as shown in figure 6.26.

The action of the Schottky in the lateral hybrid was demonstrated to ‘clamp’ the level of V_{EB} in bipolar mode and thus prevent the hole concentration in the base region rising until depletion of the emitter occurred. Otherwise, the operation of the high metal work function (Φ_M) Schottky was ‘invisible’ to the lateral hybrid in terms of bipolar conduction start up voltage (V_i) and saturation level. Whereas within an IGBT or vertical hybrid ever increasing levels of V_{EB} resulted from a positive feedback as minority carrier concentrations increased in the base. V_{EB} would reach a maximum only when conductivity modulation of the P-Anode occurred, or the MOS channel reached a maximum electron current density, at

which point the device would saturate. Due the effects of carrier concentration on V_{EB} the vertical hybrid was thus more likely to suffer from static (or dynamic) latch up when compared the lateral hybrid.

Vertical hybrid	Lateral hybrid
Bipolar start up voltage (V_i) adjusted using Schottky contact metal work function (Φ_M) and P-Anode contact length (higher Φ_M and longer P-Anode = lower V_i)	Bipolar start up voltage (V_i) adjusted using PNP BJT base width (B_W) only (lower B_W = lower V_i)
BV min = 500 V target easy to achieve if D_L adjusted to ensure $V_{PT} > 1D-BV$	BV limited by exposed P-body radius of curvature. BV min = 500 V target requires use of charge balance techniques (compromise exists between maximising V_{PT} and minimising B_W)
Unipolar conduction $R_{(ON)}$ increased by increased P-Anode length	Unhindered unipolar conduction, this structure achieves lowest unipolar $R_{(ON)}$
Reduced B_W option would not overcome hindrance of P-Anode length in unipolar mode	Reduction in B_W using N-buffer to form a lateral PT-IGBT structure yielded improved bipolar PNP BJT performance in terms of reduced V_i and $I_{A,sat}$
Emitter to base bias (V_{EB}) of the PNP BJT NOT limited by Schottky conduction (hybrid acts like NPT-IGBT in bipolar mode)	Emitter to base bias (V_{EB}) of the PNP BJT limited by Schottky conduction
Option to adjust active area of injected cells to non injected cells ratio to reduce unipolar $R_{(ON)}$, but may risk hot spot formation in bipolar mode and hence reduced ruggedness to repeated fault conditions	Option to adjust active area of injected cells to non injected cells ratio to reduce unipolar $R_{(ON)}$, but may risk hot spot formation in bipolar mode and hence reduced ruggedness to repeated fault conditions
No improvement in PNP BJT performance possible at a given BV as B_W fixed and any P-Anode extension causes degradation of unipolar conduction.	Option to adjust vertical drift length to improve PNP BJT performance, but at cost of increase $R_{(ON)}$ in unipolar mode. Increase in D_L =increase in V_{EB} (reduced V_i and increased $I_{A,sat}$)

Table 6.6. Comparison of merged injector benefits in a vertical and lateral injected hybrid structure

As summarised in table 6.6 the lateral hybrid structure offered lowest static loss in unipolar mode and greater flexibility in terms of bipolar static loss reduction. The next aspects of the hybrid design to be investigated were to assess the performance of the laterally injected hybrid as compared to an IGBT and VDMOSFET of equal blocking voltage in terms of the following: -

- 1) Establish the DC characteristic of the laterally injected hybrid at the following ambient heat sink temperatures: 233, 300 and 400 Kelvin.

- 2) Analyse the switching performance and hence dynamic loss. In particular the activation of the parasitic NPN BJT device contained within the MOS P-body was to be evaluated.
- 3) Assess the active area required to conduct a given amount of current.

6.6 References

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Chapter 7 | Semiconductor switching device performance comparison

7.0 Introduction

Previously in chapter 6 the lateral hybrid structure was demonstrated to achieve an improved PNP Bipolar Junction Transistor (BJT) performance when compared to the vertical hybrid structure of an identical cell width and drift length, and using the same merged Schottky anode. Performance improvements were in terms of bipolar start up voltage (V_i) and PNP BJT collector current level for a given on state voltage (V_{AK}). This improvement in bipolar mode was due to the reduced PNP BJT base width (W_B), but the penalty was a reduced blocking voltage performance relative to the vertical hybrid as caused by the reduced open base transistor breakdown (BV_{CEO}) as a consequence of reduced base width (W_B). Most importantly, to the aims of the device design, the lateral hybrid also provided the lowest specific on state resistance, $R_{(ON,SP)}$ during unipolar conduction mode as compared to the vertical hybrid of the same vertical drift length (D_L) as demonstrated in chapter 6.

In this chapter a direct performance comparison will be made of the lateral hybrid design to the currently available standard MOS controlled power semiconductor switching devices of an identical blocking voltage rating. The semiconductor device structures to be tested in addition to the lateral hybrid were a Non Punch Through IGBT (NPT IGBT), and a standard VDMOSFET of identical BV rating. Each semiconductor device structure utilised the same P-body design and channel geometry. The static and dynamic (or switching) performance of each device under test was to be compared in response to different ambient

heat sink temperatures. The results would be compared to the specification of an electro-mechanical contactor which was the switching device to be replaced. The tests completed on the semiconductor devices encompassed the following:-

- a) Forward blocking I-V characteristics ($V_{GK} = 0$ V) at an ambient heat sink temperature (T) of 233, 300 and 400 K (Kelvin). To confirm identical BV at $T=300$ K and assess the effect of ambient heat sink temperature on BV .
- b) Forward I-V characteristics at an ambient heat sink temperature (T) of 233, 300 and 400 K (Kelvin). To confirm static conduction loss due to the ambient heat sink temperature and to confirm the effects of resultant self heating effects.
- c) An unclamped inductive switching test of a pure inductive load was used to assess the dynamic loss associated with turn -off of the compared devices and to confirm the additional effects on self heating due an inductive load. A particular need was to establish the susceptibility to dynamic ‘latch up’ of the hybrid device.

In addition to the above, the active area of each semiconductor device to conduct 100 A (dc) was compared in order to enable any benefit to be established of using the lateral hybrid over simply using a greater VDMOSFET area, or the use of a high current to active area ratio IGBT.

Once completed the test data will then be used to identify if the lateral hybrid structure would offer any benefit over the commercially available device types, particularly with respect to the ‘mission profile’ and specification of the electro-mechanical circuit breaker (CB) replacement application within the Solid State Power Controller (SSPC) as discussed in chapter 2.

7.1 Compared structures

The compared CB device was the KILOVAC EV200 series as supplied by Tyco Electronics Corp[1]. The compared semiconductor structures utilised during this work are shown in figure 7.1. It should be noted however, that the lateral hybrid structure used during the evaluation was not optimum in terms of half cell width, as a width of $13.5\text{ }\mu\text{m}$ was utilised

incorporating a full injector structure. As shown in chapter 6, figures 6.28 and 6.29, the true optimum half cell width was 11 μm which allowed $V_{EB} = V_{BI}$ to be developed across the base to emitter junction of the PNP BJT at a lower terminal bias (V_{AK}), thus the bipolar start up voltage (V_i) was reduced when compared to the 13.5 μm wide half cell structure. The use of an 11 μm half cell width therefore would not only provide a reduced active area (thus improved $R_{(ON,SP)}$), but also provide reduced power losses (P) where $P = V_{AK} \times I_K (\text{W})$ in bipolar mode. The various performance comparison plots provided in this chapter, in units of $\text{A}/\mu\text{m}$, are therefore accurate for the structures as shown in figure 7.1. As a recommendation, ideally, for a comparison in units of A/cm^2 , and to compare the lateral device with optimum PNP performance then the work is required to be re-simulated and compared using the structure of figure 6.20 a. However, as shown in figure 7.1, a 10 μm thick vertical drift distance was used in the lateral hybrid, which from the work of chapter 6 reduced the level of V_{EB} bias at any given V_{AK} . The lateral hybrid model used therefore represented the lateral device with the lowest PNP BJT performance for a given (W_B), but the reduced vertical drift distance provided an improved unipolar performance in terms of $R_{(ON,SP)}$.

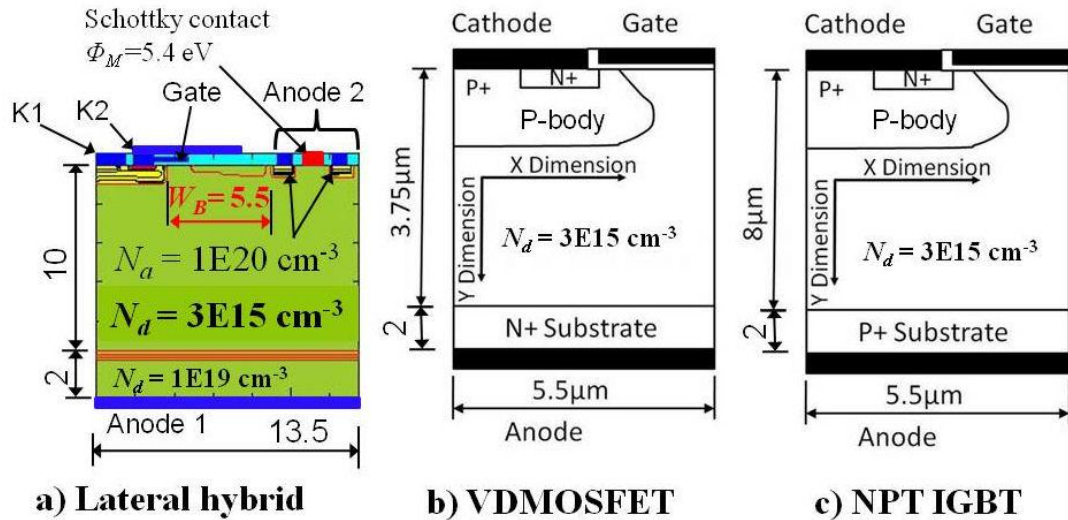


Figure 7.1. Compared MOS gated structures of approximately equal BV .

In preceding chapters all structures were modelled on an isothermal (or non self heated) basis. In order to compare the thermal performance of the structures, to include self

heating effects during both static and dynamic testing, then to each a bulk thermal resistance was added to replicate the thermal impedance of a silicon substrate of 120 μm thick as detailed in the Medici user guide, Synopsys[2]. This addition created a thermal capacitance which enabled the study of the effects of self heating in addition to the affects of altering the ambient heat sink temperature. If a reduced thickness silicon wafer is utilised (where 300 μm is the standard thickness) then more heat flux flows through the reduced thermal impedance, therefore more heat can be removed in a reduced time from the junction area, thus reducing self heating and bulk effects, hence enabling increased current flow for longer duration. In this investigation the conditions of each simulation were kept constant; with the use of a temperature and concentration dependant mobility calculation in conjunction with calculation of the current induced lattice temperature from a set fixed ambient heat sink temperature (T) of 233 K, 300 K or 400 K.

7.2 Mission profile of the electro-mechanical switch

The application review included within chapters 1 and 2 stated that the CB replacement semiconductor switch was required for the More Electric Aircraft (MEA) as was described by Rosero[3]. A summary of the mission profile and hence requirements for the CB within the SSCB as required by the MEA are summarised below in table 7.1.

Key Parameter	Requirement	EV 200 series specification[1]
Operating Voltage	270 V dc	12-900 V
Operating Ambient heat sink temperature range (T)	-40 °C to +127 °C (233 K to 400 K)	-40 to + 85 °C
Continuous current rating (fault current)	High as possible (due to use of Li-Ion batteries)	500 A at 85 °C
On state resistance	Minimum	0.2 m Ω (at 200 A dc)
Fault break current	High as possible	2000 A (at 320 V)
BV	Maximum possible (500 V min)	2200 V _{RMS}
Switch off time	Minimum possible	12 ms (at 2000 A)
Switching frequency	Sporadic switch events only	<66 Hz ($F=1/t_{on}$)
Turn off energy	Lowest	Limited by arcing
Predominant load	Inductive + stray capacitance	Inductive + stray capacitance

Table 7.1. Summary of switch requirements within the SSPC of an MEA shown in relation to an electro mechanical switch.

A typical ‘mission profile’ of an SSPC, utilised within the power distribution system of an MEA would encompass both low and high ambient heat sink temperature extremes $T=233\text{ K}$ to $T=400\text{ K}$, though currently this is limited by the CB technology to $+85\text{ }^{\circ}\text{C}$ (358 K). Convection only cooling from a non infinite heat sink would lead to the devices tending to operate predominantly at higher ambient heat sink temperatures. Although the operating voltage is shown in table 7.1 as 270 V dc (hence the required minimum $BV=500\text{ V}$), then as explained earlier in chapter 2, during this investigation the proof of hybrid concept was to be evaluated in this work with a $BV\approx 100\text{ V}$.

7.3 Forward blocking performance

Corresponding to the proof of concept $BV\approx 100\text{ V}$ described above, the resultant forward blocking performance of each of the compared semiconductor structures of figure 7.1 are shown in figure 7.2. As can be seen the blocking voltage, at $T=300\text{ K}$, of each of the compared structures was equalised at around $BV = 84\text{ V}$. Each structure was simulated using

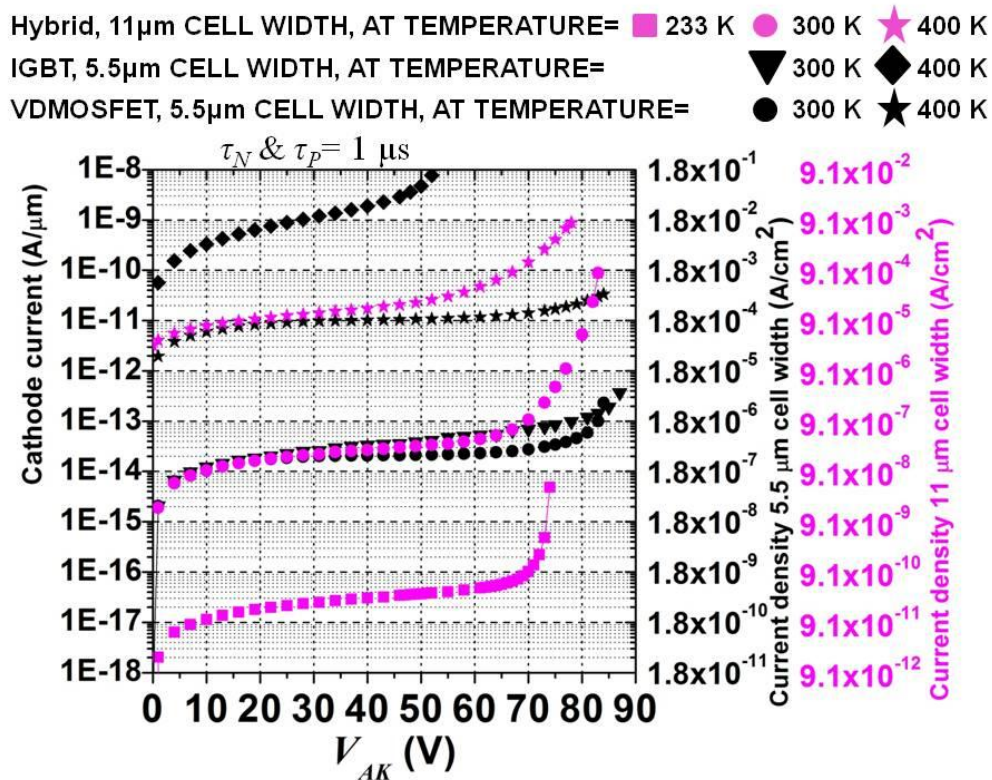


Figure 7.2. A blocking capability comparison of the structures as shown in figure 7.1 at various ambient heat sink temperatures.

a template program adjusted only to change the ambient heat-sink temperature of $T=300$ K and 400 K with $V_{GK}=0$ V, stepping V_{AK} up from 0 V, in 1 V increments, until conduction was evident. The hybrid was also simulated at $T=233$ K.

Within the lateral hybrid at $T=233$ K the $BV=74.5$ V which was lower than that at room temperature. This is in agreement with Sze[4] who stated that the avalanche breakdown in a reverse biased (1-D) abrupt P-N junction at $T=233$ K would be lower than at room temperature. The level of leakage current at $T=233$ K was also lower than that at $T=300$ K due to the change in the Fermi level and hence increased V_{BI} of the emitter to base junction of the integral PNP BJT.

With reference to figure 7.2, the progressively increased leakage current (J_L) of the lateral hybrid and NPT IGBT with increased V_{AK} as compared to the VDMOSFET (at $T=300$ K) was due to the extension of the PNP BJT collector–base depletion region. The neutral base width that carriers must diffuse across was therefore also decreasing, therefore the amplification of the space charge generated current (J_{SCG}) also increased due to increased base transport factor (α_T) in line with the effect described by Early[5]. Equations 7.1 and 7.2 describe the relationship between J_L and J_{SCG} as described by Baliga[6].

$$J_L = \frac{J_{SCG}}{1 - \alpha} \quad (7.1)$$

$$J_{SCG} = \frac{qW_D n_i}{\tau_{SC}} = \frac{n_i}{\tau_{SC}} \sqrt{\frac{2qK_s \epsilon_O V_{AK}}{N_d}} \quad (7.2)$$

Where $U = \frac{n_i}{\tau_{SC}}$ = space charge generation and τ_{SC} is the space-charge generation lifetime.

The leakage current (J_L) at an ambient heat sink temperature of 400 K was significantly larger than at 300 K because the intrinsic carrier concentration (n_i) increases by approximately two orders of magnitude ($1E10$ to $2E12$ cm⁻³) between room temperature and 127 °C (400 K) as described by Grove[7] and Sze[4]. In addition the temperature dependant shift in Fermi level of the emitter to base junction, as described by Grove[7], caused an

increase in the leakage level relative to the VDMOSFET of both the lateral hybrid and particularly the NPT-IGBT.

Within the NPT-IGBT the reduction in the traversed distance together with the higher generation rate within the larger collector -base depletion region extent forms a cumulative effect for increased leakage current with increased levels of forward voltage drop (V_{AK}). The leakage levels and gain affect the open base transistor breakdown (BV_{CEO}) as described by Sze[4] and Baliga[6] and formed the reason why at $T = 400$ K the forward blocking voltage of the IGBT was reduced to approximately 47 V as punch through had not occurred.

7.4 Forward conduction performance comparison

Having established that the compared semiconductors were of identical blocking voltage at $T=300$ K, in this section a direct comparison of the forward conduction characteristics could be provided. With use of a fixed gate bias ($V_{GK}=20$ V) on each of the compared structures, the effect of altering the ambient heat sink temperature for each device will also be described under static conduction conditions only. The ambient heat sink temperature and junction temperature are identical at initiation of the simulation, however the static losses during conduction of the device, due to the instantaneous dissipated power (P) where $P = V_{AK} \times I_K$ (W), cause self heating to the lattice and hence the lattice temperature can rise locally above that of the heat sink as described by Swan[8]. All manufacturers therefore would specify a maximum junction temperature due directly to the static loss which forms the upper safe operational limit for the device, as described by a Safe Operating Area curve (SOA) which varies with ambient heat sink temperature, and duty cycle (if switched).

7.4.1 Experimental method to assess temperature performance

To compare the performance of each of the structures as shown in figure 7.1 over changes in the ambient heat sink temperature, then a fixed gate bias of $V_{GK}=20$ V was used to ensure bipolar activation in the lateral hybrid. For each structure to be compared the conditions of the simulation were unchanged and a template program was used for each. After setting the initial ambient heat sink temperature (T) the terminal bias (V_{AK}) was then increased in 0.05 V steps.

7.4.2 Results of forward I-V characteristics with temperature effects

The effect of temperature on the forward conduction characteristic of each structure is shown as direct comparison in figures 7.3 and 7.4. The resultant lattice temperature contour plots as shown in figure 7.5 were taken at the maximum simulated current at each initial ambient heat sink temperature setting of the lateral hybrid.

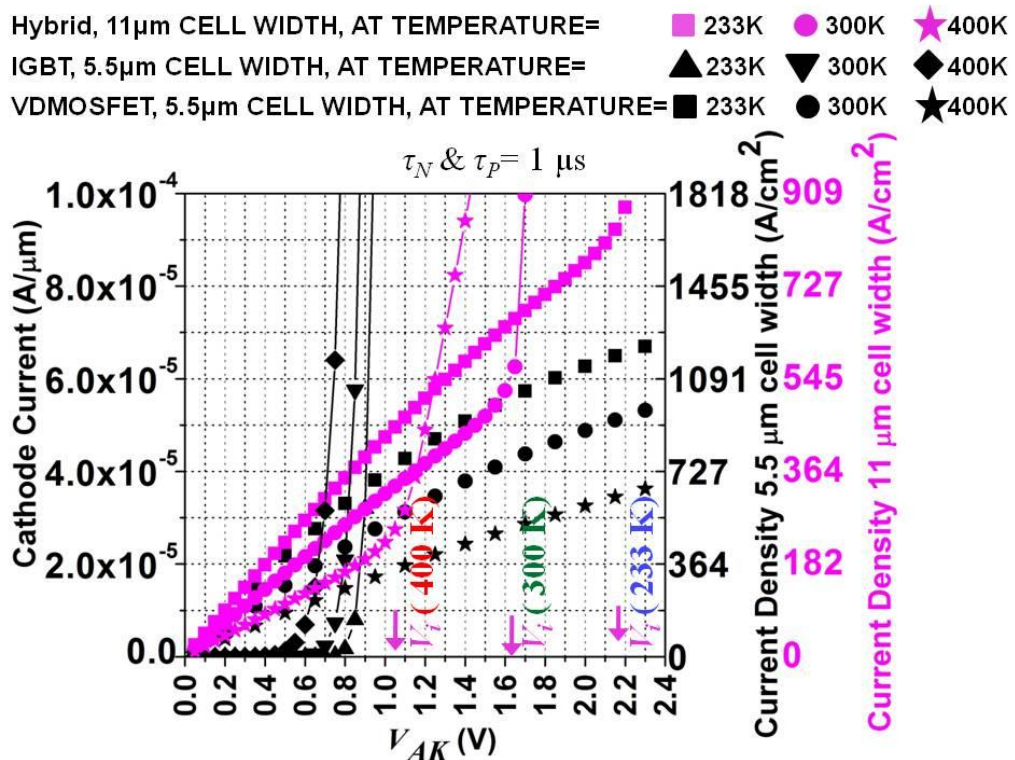


Figure 7.3. Zoomed comparison of forward conduction characteristics of each structure from figure 7.1 at three ambient heat sink temperatures:- a) 233 K, b) 300 K and c) 400 K.

Hybrid, 11 μ m CELL WIDTH, AT TEMPERATURE= ■ 233K ● 300K ★ 400K
 IGBT, 5.5 μ m CELL WIDTH, AT TEMPERATURE= ▲ 233K ▼ 300K ◆ 400K
 VDMOSFET, 5.5 μ m CELL WIDTH, AT TEMPERATURE= ■ 233K ● 300K ★ 400K

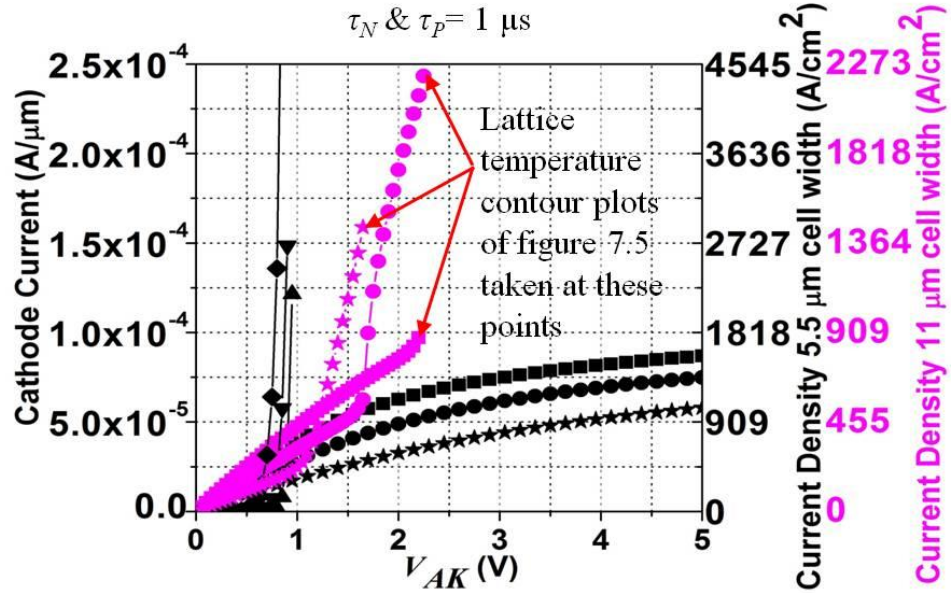


Figure 7.4. Full scale comparison of forward conduction characteristics of each structure from figure 7.1 at three ambient heat sink temperatures:- a) 233 K, b) 300 K and c) 400 K.

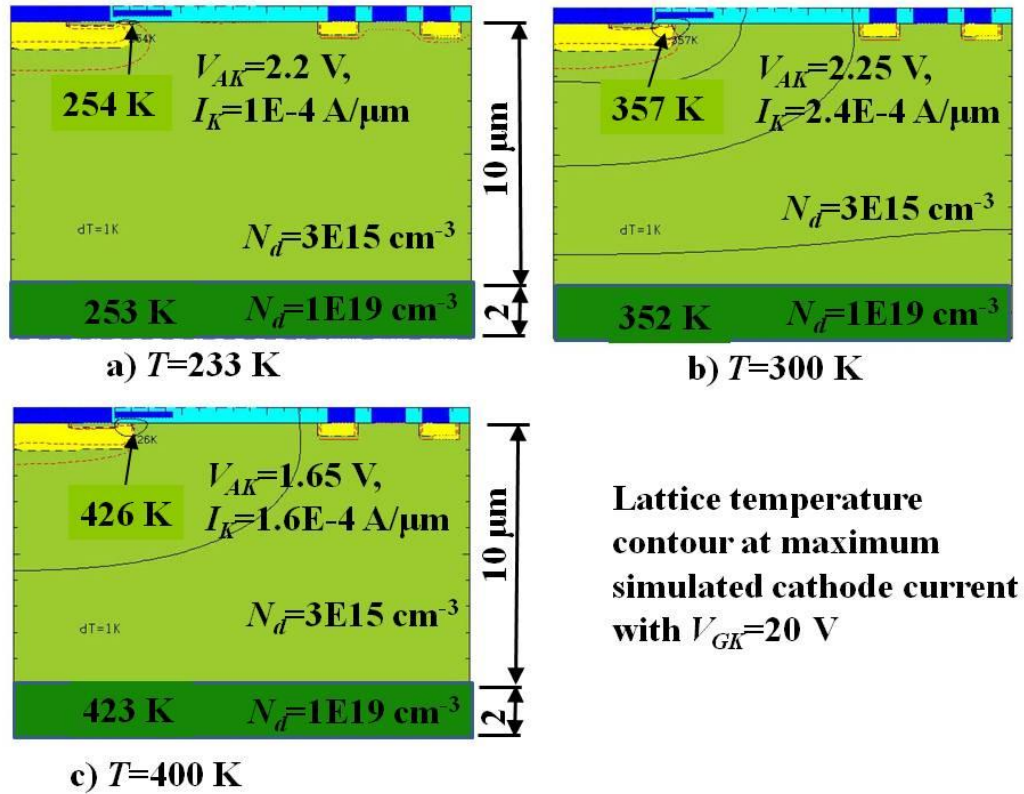


Figure 7.5. Comparison of instantaneous lattice temperature contour plots at three ambient heat sink temperatures:- a) 233 K, b) 300 K and c) 400 K.

7.4.3 Effects of localised heating due to instantaneous power loss

The lattice temperature contour plots of figure 7.5 showed the resultant temperature contours within the lateral hybrid at the maximum simulated current level at a given initial ambient heat sink temperature as shown in figure 7.4. The highest point of lattice temperature was around the channel area under the gate electrode due to the high current density. This is an identical situation for the VDMOSFET as this point coincides with the high carrier density in the inversion layer and accumulation region. Indeed, this was also validated by the work of Pendharkar[9], Trivedi[10, 11] in relation to the IGBT.

With regard to figure 7.5 the addition of the thermal resistance to the substrate had meant that the temperature at the N-Drift region to substrate junction has also increased over and above the heat sink ambient temperature. In the bipolar mode of the lateral hybrid at $T=300$ K and $T=400$ K (figure 7.5 b and c) then the top of the substrate was approximately at a temperature of 50 K over and above the initial ambient heat sink temperature. This provided an indication of how the added thermal impedance to replicate a 120 μm thick silicon substrate restricted the heat flux and hence heat would build up in the device due to static power loss.

7.4.4 Effects of heating on the MOS channel

Each of the compared structures of figure 7.1 had in common the same effects of temperature on the threshold voltage (V_{TH}) of the MOS channel because the same P-body and gate design was common to all and were subject to the localised lattice temperature high point. As the localised temperature in the channel area increased, the effect was to reduce the threshold voltage (by approximately 0.2 to 0.4 V) due to the $2\psi_B$ terms in equation 7.3, and the converse also applied, as defined by Grove[7].

$$V_{TH} = \frac{\sqrt{2K_S \epsilon_O q N_a 2\psi_B}}{C_{OX}} + 2\psi_B - \frac{Q_{OX}}{C_{OX}} \quad (\text{V}) \quad (7.3)$$

In addition the saturation transconductance (g_{ms}) of the MOS channel would also reduce with increased junction temperature, due the reduction of the inversion layer mobility (μ_{ni}). Where μ_{ni} decreases with temperature and reduces with concentration as n_i increases with increasing temperature. All of which negates any benefit of threshold voltage (V_{TH}) reduction within equation 7.4, again as described by Baliga[6]. The reduction in saturation level is clearly

$$g_{ms} = \frac{Z\mu_{ni}C_{OX}}{L_{CH}}(V_{GK} - V_{TH}) \quad (7.4)$$

evident in the VDMOSFET characteristics with increasing temperature as shown in figures 7.3 and 7.4. Under high junction temperature conditions the effect of the reduced saturation level (g_{ms}) would mean that in a high load or fault current event the VDMOSFET would enter the high resistance, or ‘saturated’, state at a much lower current level than when the ambient heat sink temperature was low at a given gate bias level. The implication of the low saturation level at $T=400$ K is that the active area of VDMOSFET must therefore be large enough to ensure that any possible fault current could be safely conducted (without entry into the saturation state and hence operate inside of the SOA) or risk thermal failure of the VDMOSFET device.

On examination of the characteristics in figures 7.3 and 7.4 the VDMOSFET was shown to exhibit a positive temperature coefficient as described by Baliga[6], in that the on state resistance of the device increased with increased junction temperature as indicated by the rise in terminal voltage (V_{AK}) at a given current level as temperature is increased. This rise in voltage with temperature was due to mobility affects, wherein the mobility decreased and hence resistance increased with increasing device temperature. The behaviour of the lateral hybrid in unipolar conduction mode as shown in figures 7.3 and 7.4 was to behave in the identical manner of the VDMOSFET for the above reasons. The IGBT had no unipolar conduction mode and therefore only incurred a static power loss once bipolar conduction began following activation of the P+ Anode, or emitter of the integral PNP BJT, when $V_{AK} = V_i$.

7.4.5 Effects of temperature on bipolar conduction

The effect of an increase in the junction temperature of the NPT IGBT was to decrease the on state voltage drop due to a reduction in the bipolar start up voltage (V_i), or the ‘knee’ in the characteristic, in terms of V_{AK} bias as shown in figures 7.3 and 7.4. This was not only due to the reduction in V_{TH} , but also due to the increased intrinsic carrier concentration (n_i) and thermal voltage (kT/q) which serve to decrease the required voltage (V_{EB}) to overcome the emitter to base potential barrier (V_{BI}) of the internal PNP BJT as calculated using equation 7.5.

$$V_{BI} = \frac{kT}{q} \ln \left[\frac{N_a N_d}{n_i^2} \right] \quad (7.5)$$

Khanna[12] argued that the NPT IGBT had a negative temperature coefficient of resistance as he stated that current would fall with increasing temperature. However, this is not in agreement with figure 7.3 as clearly at $V_{AK}=0.7$ V the current increased with increased temperature if a comparison is made between $T=300$ K and $T=400$ K, this was due to the change in bipolar turn on voltage (V_i). The on state resistance of the NPT IGBT device therefore fell with increasing temperature, if the signing of the temperature coefficient of resistance was in line with that of the VDMOSFET as described by Baliga[6], then the temperature coefficient of resistance was indeed negative as stated by Khanna. In a situation where the IGBT and the VDMOSFET were conducting in parallel, then if a large increase in the lattice temperature occurred, due for example to a sudden increase in static power loss due to fault current, then the NPT IGBT would conduct an increasing amount of current share, whereas the VDMOSFET would saturate at a current level dictated principally by the active area, but also the lattice temperature and resulting mobility. Subsequent to bipolar start up at voltage (V_i) in terms of V_{AK} , the IGBT therefore could protect a parallel VDMOSFET from thermally induced catastrophic failure by clamping the voltage across the

parallel VDMOSFET, thus preventing VDMOSFET saturation. A similar effect occurred within the lateral hybrid.

The effect of increasing junction temperature on the lateral hybrid device was essentially the same as the NPT IGBT, however; the effect of the reduction in the bipolar start up voltage (V_i) or ‘knee’ was much more pronounced than with the NPT IGBT, due to the vertical and lateral electron conduction paths. At high temperature the resistance of the vertical electron conduction path to anode 1 increased due to decreasing mobility, the voltage V_1 therefore was increased in the same way as the VDMOSFET. With reference to the work of chapter 5, particularly figures 5.21, 5.22 and 5.23, the increase of V_1 meant that the voltage V_4+V_3 was also increased due to equality. Wherein $V_{EB}=V_3$, therefore V_{EB} was also increased at high temperatures relative to cold temperatures and yet the base to emitter junction potential barrier (V_{BI}) simultaneously decreased within the internal PNP BJT due to the described high temperature effects on equation 7.5, thus V_i decreased with increased temperature. Of the bipolar enabled structures then the NPT IGBT achieved the lowest V_i and hence highest current for lowest on state voltage, thus lowest static loss, at all ambient heat sink temperatures.

7.4.6 Summary of static performance over temperature

With use of the forward static I-V data in units of A/ μm and V from figure 7.4, a direct comparison of the active area (A) required to conduct $I_K=100$ A and the specific on state resistance, $R_{(ON,SP)}$, can be directly compared at each of the ambient heat sink temperatures tested as shown in figures 7.6 to 7.8, (at $T=400\text{K}$, $T=300\text{K}$ & $T=233\text{K}$ respectively). The active area of each half cell structures was as per figure 7.1, noting that for the lateral hybrid in the calculations a half cell width of 11 μm was used (not 13.5 μm) as 11 μm reflected the true half cell structure as shown in chapter 6, figure 6.20 a) albeit that the structure of figure 7.1 a) did not benefit from the improvement in V_{EB} made possible in the structure of figure 6.20 a). The active area required to conduct 100 A, utilised a scale factor of 100 A/the simulated current (in A/ μm) at each voltage step (from figure 7.3). The area required for 100

A was therefore the half cell area ($1\text{E-}4 \times 11\text{E-}4$ cm in the case of the hybrid) x the scale factor. From that data the instantaneous power density could also be calculated.

Due to the positive coefficient of resistance the active area of the VDMOSFET, required within the SSPC application must be sized to conduct the anticipated fault current within the linear region of operation at $T=400$ K. The NPT-IGBT and the lateral hybrid active area, due to the reduction in V_i with increasing temperature, would need to be sized to conduct the anticipated fault current at $T=233$ K which represents the highest static loss. If the lateral hybrid was utilised then the active area required to conduct the fault current in comparison to a VDMOSFET solution can be approximately halved (at $T=400$ K, $V_{AK}=1.65$ V and $T=300$ K, $V_{AK}=2.15$ V). At $T=233$ K, as shown in figure 7.8, then the restricted data points do not show the bipolar performance to allow a comparison.

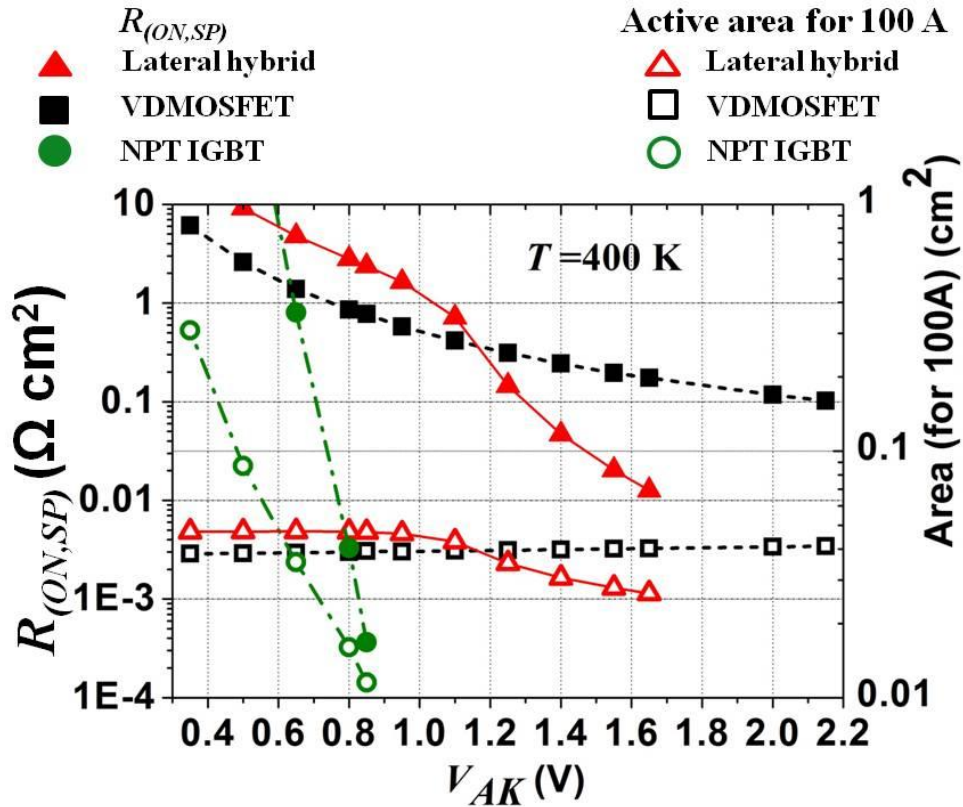


Figure 7.6. Direct comparison of $R_{(ON,SP)}$ and active area required to conduct 100 A at ambient heat sink temperature of $T=400$ K.

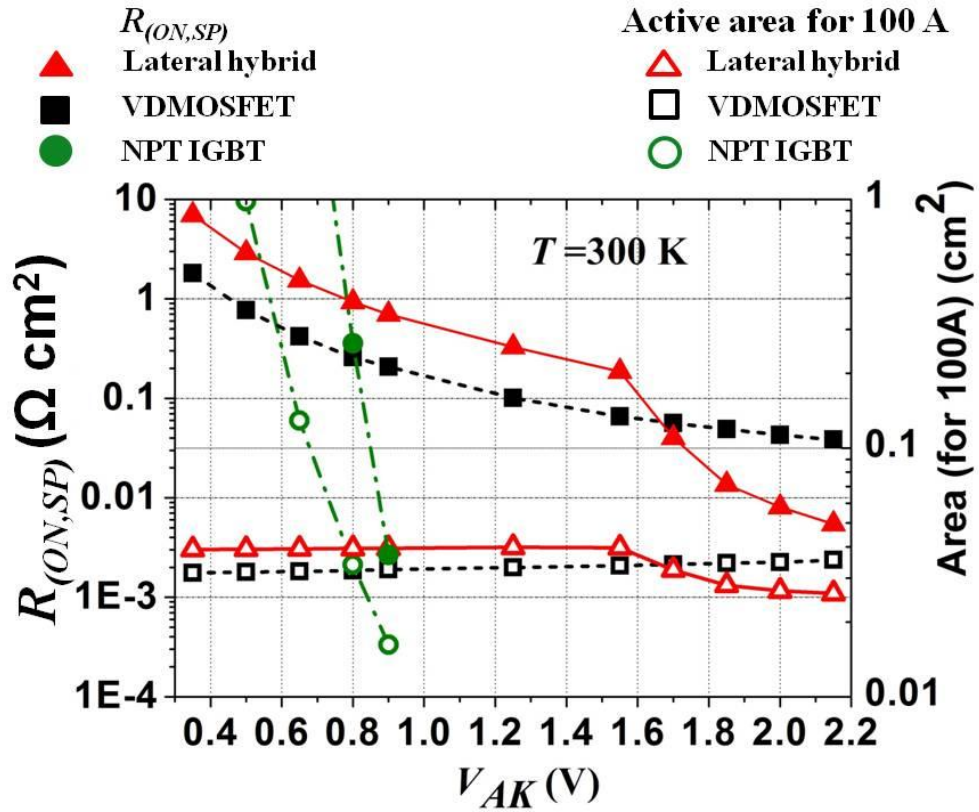


Figure 7.7. Direct comparison of $R_{(ON,SP)}$ and active area required to conduct 100 A at ambient heat sink temperature of $T = 300$ K.

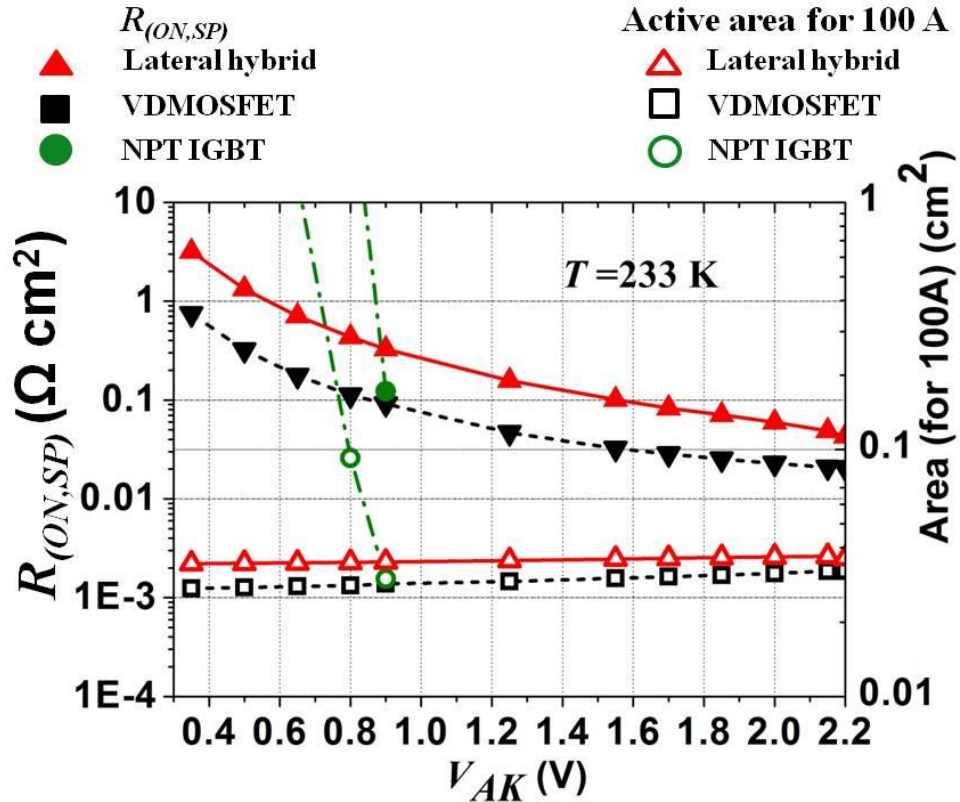


Figure 7.8. Direct comparison of $R_{(ON,SP)}$ and active area required to conduct 100 A at ambient heat sink temperature of $T = 233$ K.

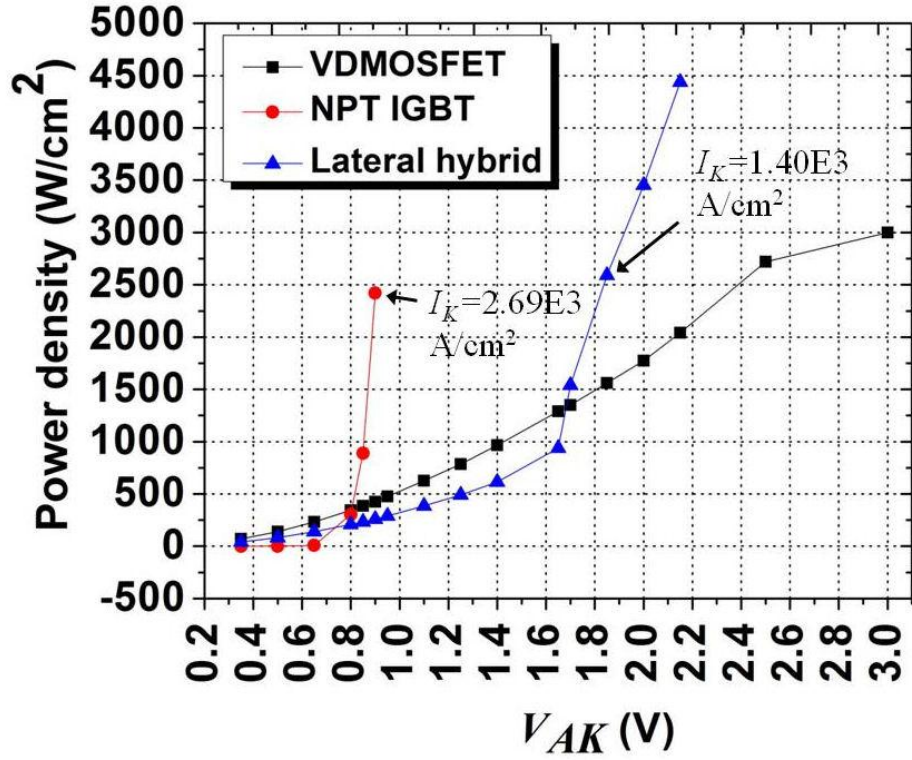


Figure 7.9. Plot of static power density versus V_{AK} (at $T=300$ K for structures of figure 7.1).

Clearly from figures 7.6 to 7.8 the NPT-IGBT, at all temperatures, offers the lowest active area and lowest $R_{(ON,SP)}$ when compared to the lateral hybrid and VDMOSFET. The resulting reduced static losses expressed in terms of power density, as shown in figure 7.9, clearly demonstrate the increased current conducting capability of the NPT-IGBT as compared to the lateral hybrid. However, the hybrid, like the VDMOSFET, allows a controllable current flow from $0 \text{ V} < V_{AK} \leq 0.1 \text{ V}$, whereas with the IGBT the current flow begins at $V_{AK} \approx 0.8 \text{ V}$. At $V_{AK} = 2 \text{ V}$ in bipolar mode the lateral hybrid shows an improvement over the VDMOSFET as $R_{(ON,SP)} = 1.16 \text{ m}\Omega\text{cm}^2$, which has clearly broken the 1-D silicon limit line, as described by Hu[13]. The dynamic losses of the comparison devices therefore now need to be assessed in order to choose the device type with the lowest losses under all conditions.

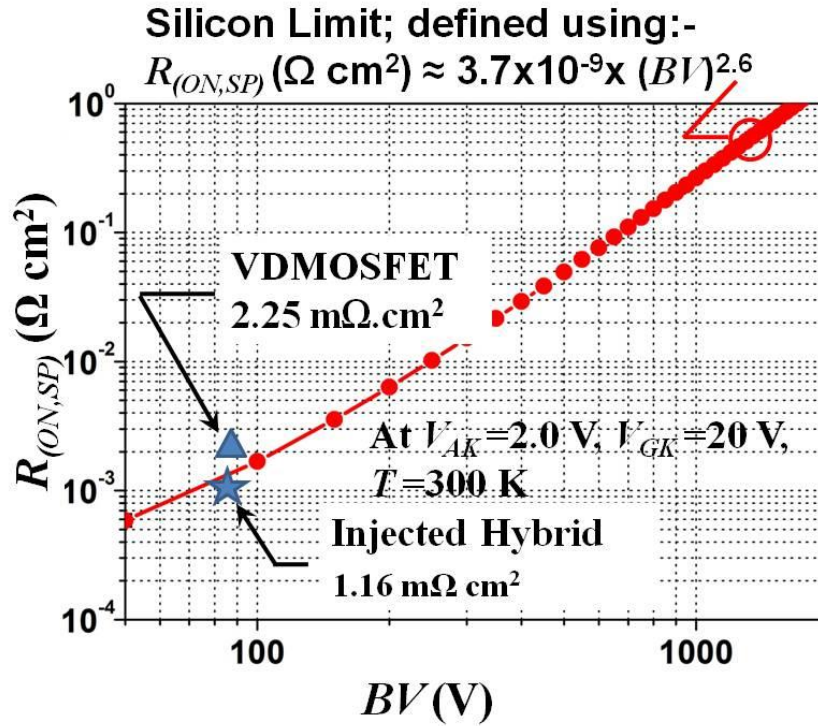


Figure 7.10. Direct comparison of the lateral hybrid and VDMOSFET in relation to the calculated silicon limit line (Baliga[6]) at ambient heat sink temperature of $T = 300 \text{ K}$.

7.5 Unclamped inductive switching performance

Having evaluated the effects of ambient heat sink temperature on the static, or dc, characteristics, in this section the investigation into the effects of temperature on the dynamic switching characteristics is reported. As the potential loads were to be predominantly inductive in nature the unclamped inductive switching test (UIS) was therefore adapted for this investigation. The UIS test is commonly used in industry to evaluate the avalanche breakdown and reverse recovery time of any given semiconductor switching device, the importance of which as regards a VDMOSFET are described by McDonald[14]. A typical standard in use is as described by the JEDEC organisation[15].

The aim of the testing was to establish the switch off time of current supplied to a pure fixed inductance load (no resistance) via the compared semiconductor device structures of figure 7.1. The susceptibility to dynamic ‘latch up’ via activation of the parasitic NPN BJT was also to be established for each structure. The ‘latch up’ condition described the loss of gate control in a conducting IGBT due to thyristor action. This affected IGBT type

devices in the early years of availability, but the risk of latch up has since been minimised by various design measures as described by Langdon[16] and Baliga[6] which included reduced N+ cathode doping width, increased P-body acceptor doping and inclusion of a highly doped cathode short for vertical hole conduction to by-pass the N+ cathode (or N+ emitter of the NPN BJT).

7.5.1 Unclamped inductive switching test method

The aims of the UIS test were to utilise a set value of inductive load, (in this case 0.9 mH) conducting a set current level (I_K) to store energy which upon incidence of switch off would force the switching device under test (DUT) to increase the voltage across the reverse biased junction (P-body to N-Drift) as described by Hummert[17] and the effect of which is shown in figure 7.11. The stored inductive energy due to I_K essentially acted to ensure the current supplied via the DUT was continued at the same level despite the DUT trying to switch –off and in doing so increasing its resistance. This lead to a high dynamic loss as the

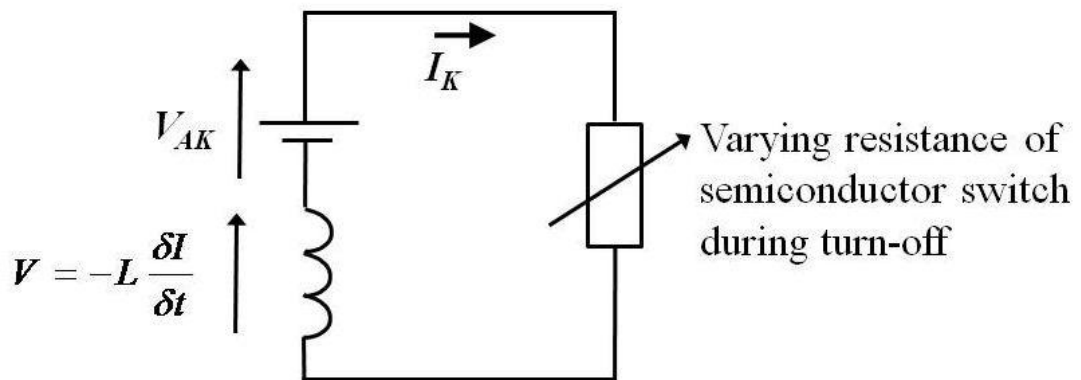


Figure 7.11. Effect of inductive load on voltage across the switch during turn off.

inductive energy led to high currents coinciding with the increasing voltage across the DUT and hence to the possibility of extremely high instantaneous power dissipation causing localised lattice heating particularly in the channel region under the gate electrode.

In this case the initial current level through the DUT into the load was defined by the terminal voltage as shown in figure 7.4, wherein V_{AK} was set to provide a high magnitude

current flow via bipolar mode within the lateral hybrid as shown in figure 7.4 with $V_{GK}=20$ V. The conduction current used through each DUT is shown in table 7.2. The gate was ramped down from $V_{GK}=20$ V to zero within a time period of $t_{fall}=2$ ns, ramp down began at $t=2$ ns after conduction began at $t=0$. The inductance value of 0.9 mH was chosen to ensure that the current flowing through the VDMOSFET at $V_{AK}=2$ V, ($T=300$ K) did not avalanche. Therefore the switching time of the VDMOSFET did not include a recovery period to equilibrium from the resultant generated carrier pairs (U) from within the space charged region of the P-body to N-Drift junction.

Structure	cathode current (I_K) (A/ μ m)	Terminal bias (V_{AK}) (V)
NPT IGBT ($T=300$ K)	1.5E-4	0.9
VDMOSFET ($T=300$ K)	6.25E-5	2.0
Lateral hybrid ($T=300$ K)	2E-4	2.0
Lateral hybrid ($T=400$ K)	1.6E-4	1.6

Table 7.2. Starting current level through the inductor for each structure during the unclamped inductive switching test (at $V_{GK}=20$ V).

Unfortunately, I-V data for the lateral hybrid in bipolar mode at $T=233$ K was not available as the simulation failed to converge due to the high dI_K/dV_{AK} at V_i . The comparative DUT test was therefore only completed at an ambient heat sink temperature of $T=300$ K, in addition the lateral hybrid was also tested $T=400$ K to evaluate the effect of ambient heat sink temperature on switching performance. It was anticipated that if latch up was to occur within the lateral hybrid then this would happen at $T=400$ K due to the increased resistance of the PNP BJT collector and decrease in V_{BI} of the N+ cathode to P-body (N+ emitter to P base of the NPN BJT) as described by Grove[7]. In addition to evaluate the worst case scenario the carrier lifetimes were set as $\tau_N = \tau_P=100$ μ s, thus the time to recombine was increased and hence recovery to equilibrium was delayed.

7.5.2 Unclamped switching test results at $T = 300\text{ K}$ and $T = 400\text{ K}$

A direct comparison of the switching performance of the VDMOSFET and the lateral hybrid tested at $T = 300\text{ K}$ are shown in figure 7.12 which include a schematic of the test circuit. In order to provide a comparison to the result at $T = 300\text{ K}$ of figure 7.12 a plot of the switching performance of the lateral hybrid tested at $T = 400\text{ K}$ is shown in figure 7.13 which again includes a schematic of the test circuit. Please note that the turn off event for the NPT IGBT could not be shown on the same time scale as shown in figure 7.12 due to the long tail current resulting from extended hole conduction which meant that the time to recovery was greater than $10\text{ }\mu\text{s}$. The voltages V1 and V2 as shown in figure 7.12 are those developed across the reverse biased collector –base, or P-body to N-Drift region, junction of the lateral hybrid and VDMOSFET respectively due to the stored inductive charge in the load. For the lateral hybrid three dimensional plots of both the electron current density and hole current density are shown in figures 7.14 and 7.15 respectively. The magnitude of the current density is shown on the Z axis relative to the cross sectional area of the half cell on the X and Y axes.

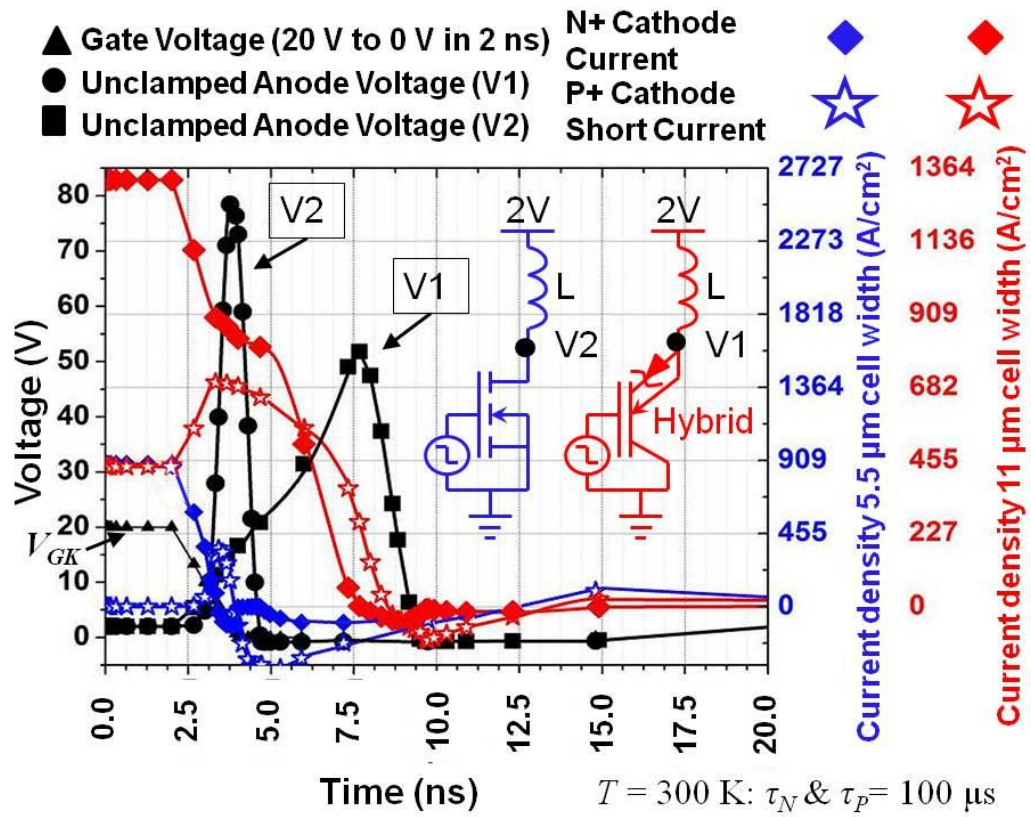


Figure 7.12. Comparison of unclamped inductive switching test at $T=300 \text{ K}$ completed on: a) the VDMOSFET and b) the lateral hybrid.

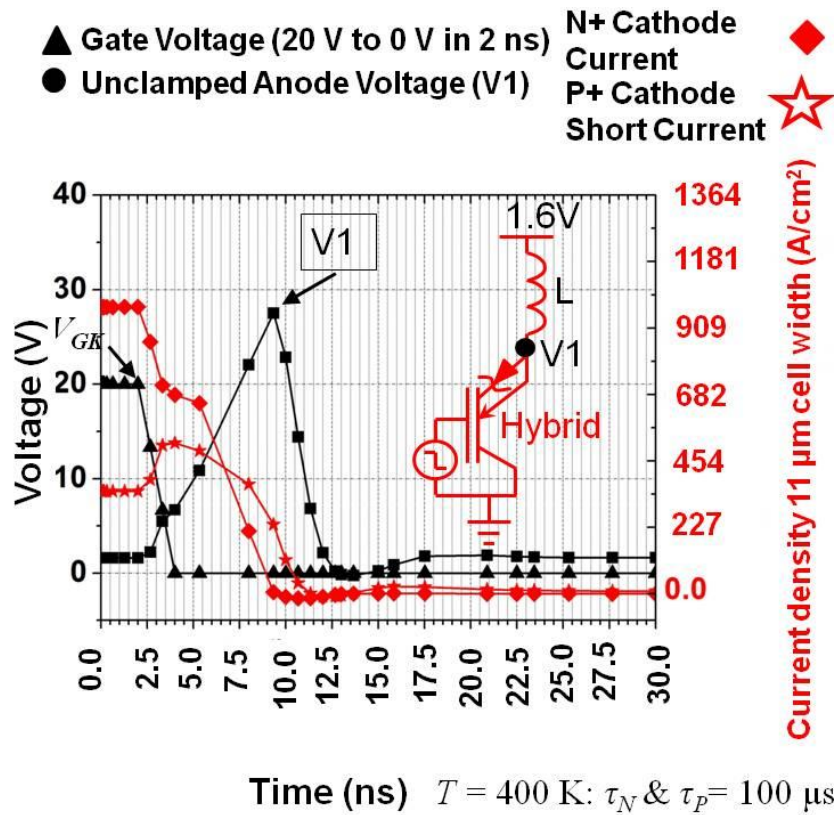


Figure 7.13. Unclamped inductive switching test completed at and ambient heat sink temperature of $T = 400 \text{ K}$ on the lateral hybrid.

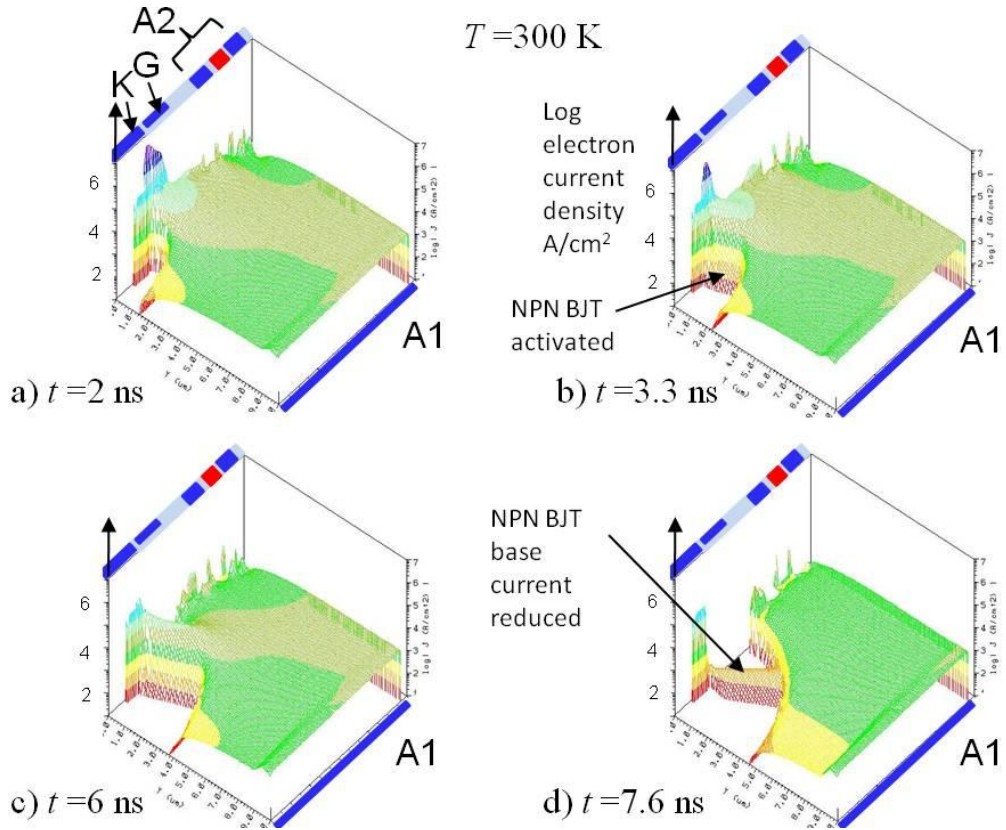


Figure 7.14. Three dimensional plots of electron current density at various times during lateral hybrid switch off (figure 7.12).

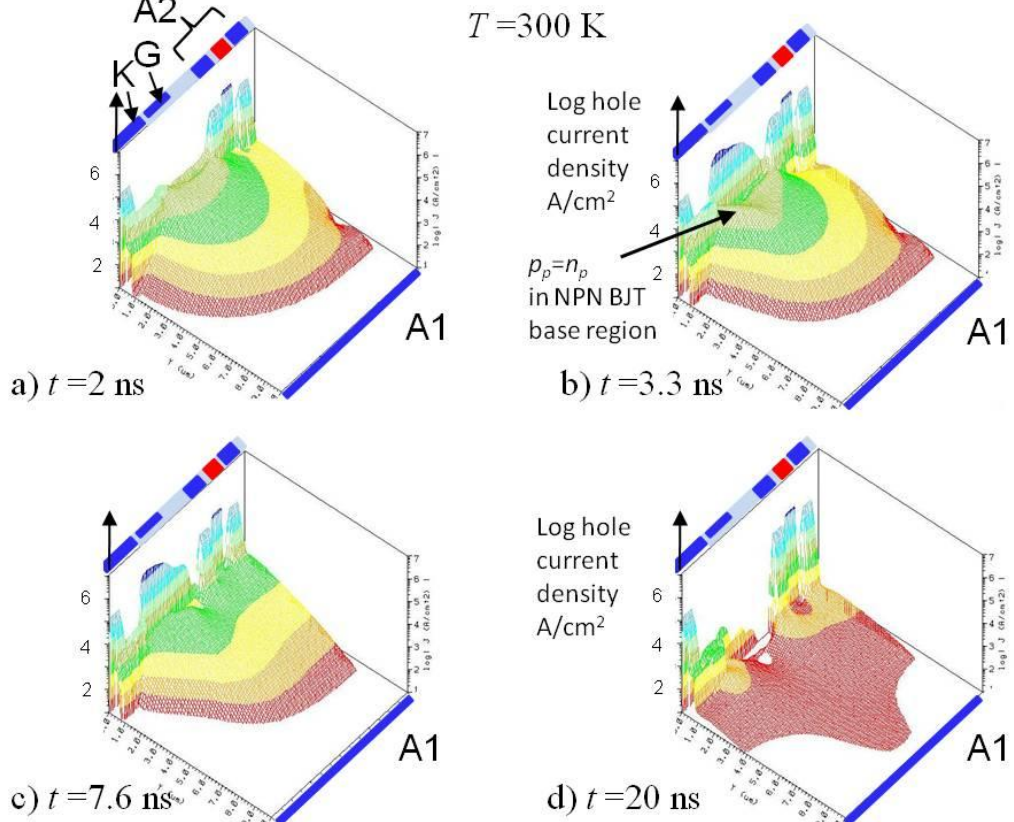


Figure 7.15. Three dimensional plots of hole current density at various times during lateral hybrid switch off (figure 7.12).

7.5.3 Discussion of test results

As shown in figure 7.12 the VDMOSFET was very close to avalanching as the forward BV of the each device under test was approximately 84 V at $T=300$ K. The current level (≈ 909 A/cm² at $V_{AK}=2$ V) prior to gate ramp down was therefore not sufficient to enter avalanche in this case with the inductance value tested, where $L=0.9$ mH. The VDMOSFET therefore safely turned off the inductive load, and the resultant power density equated to the voltage, V_2 (V) multiplied by the total current (A/cm²) during the period of the switching event.

The results of the lateral hybrid (also shown in figure 7.12) demonstrated that the increased current conducted via the lateral hybrid (≈ 1819 A/cm² again at $V_{AK}=2$ V) in bipolar mode resulted in a much larger reverse bias voltage developed across the collector to base junction during turn off using $L=0.9$ mH. This voltage however, was restricted from rising to its potential value due to the conduction through the device, which ‘self clamped’ the lateral hybrid device as follows:- The trace of red stars in figure 7.12 indicated the hole current conducted via contact K1, whereas the trace of red diamonds showed the electron current conducted via contact K2 (as shown in figure 7.1 a). At time $(t) = 2$ ns, on the x axis, the gate began to ramp down from a total current of 1819 A/cm² through the lateral hybrid. The electron current immediately began to fall, therefore the hole current increased to compensate in order to maintain the current through the inductor. At approximately time $(t) = 2.65$ ns the gate voltage fell below V_{TH} at which point the hole current reached a peak and subsequently began to fall. The preceding hole current level however, was high enough to activate the parasitic NPN BJT and hence the electron current achieved a plateau level. However, conduction of the NPN BJT was not sustained and the electron current thereafter fell simultaneously with the hole current, with V_1 rising as carrier current decreased.

The three dimensional plots of the electron and hole current densities within the lateral hybrid at a selection of time periods during the UIS test event can be seen in figures 7.14 and 7.15 respectively. The action of the parasitic NPN BJT was identified at the separate time intervals, but was first evident at time $(t) = 3.3$ ns which coincides with the hole

current peak. The conduction of the NPN BJT was not sustained as could be seen in figures 7.14 and 7.15 as the NPN base current had reduced by $t=7.6$ ns (figure 7.14d), hence the hole current diminished as shown in figure 7.15 d.

The reason why the NPN BJT conduction was not sustained in the lateral hybrid can be described with the aid of Figure 7.16 in which the equivalent circuit of the lateral hybrid is provided, identifying both the desired PNP BJT (T_{R1}) and the parasitic NPN BJT (T_{R2}). Once the gate began to ramp down, the hole current rose to compensate for the reduced electron current, thus activating T_{R2} as described earlier. The voltage V1 increased to a peak at $t=7.6$ ns due to the inductive energy as shown in figure 7.12. The corresponding band diagrams of the NPN and PNP BJTs shown in figure 7.16 are provided in relation to the peak voltage (V1) at $t=7.6$ ns.

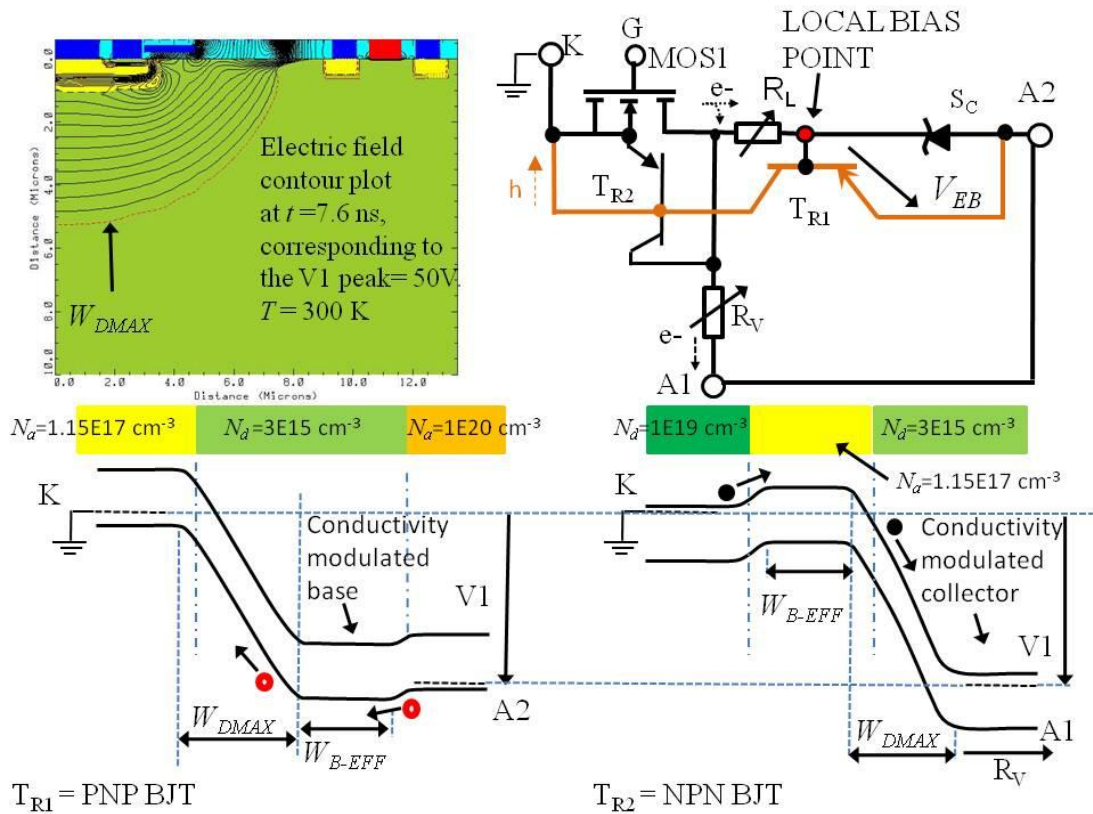


Figure 7.16. Effect of reverse bias depletion extent on PNP and NPN BJT devices inherent within the lateral hybrid.

The effective base width (W_{B-EFF}) of both T_{R1} and T_{R2} was varied with the depletion extent (W_D) which changed over the period of the switching event as indicated by voltage V1. The result of which was to vary the base transport factor (αT), and hence gain (α and β)

of each transistor, in accordance with the Early effect, Early[5]. The plateau in the hole current and hence the electron current following NPN BJT activation between $t = 3.125$ and 5 ns as shown in figure 7.12 was caused by the reduced W_{B-EFF} of the PNP BJT however, the effect of the PNP BJT base width reduction also provided increased base drive (hole current ($I_{diff,B}$) to the NPN BJT base. When the voltage V1 began to fall then W_{B-EFF} of the PNP BJT widened, thus the electron current fell sharply due to the reduced gain of T_{R1} which de-biased the emitter to base junction of the NPN BJT, thereafter both the hole and electron currents fell sharply.

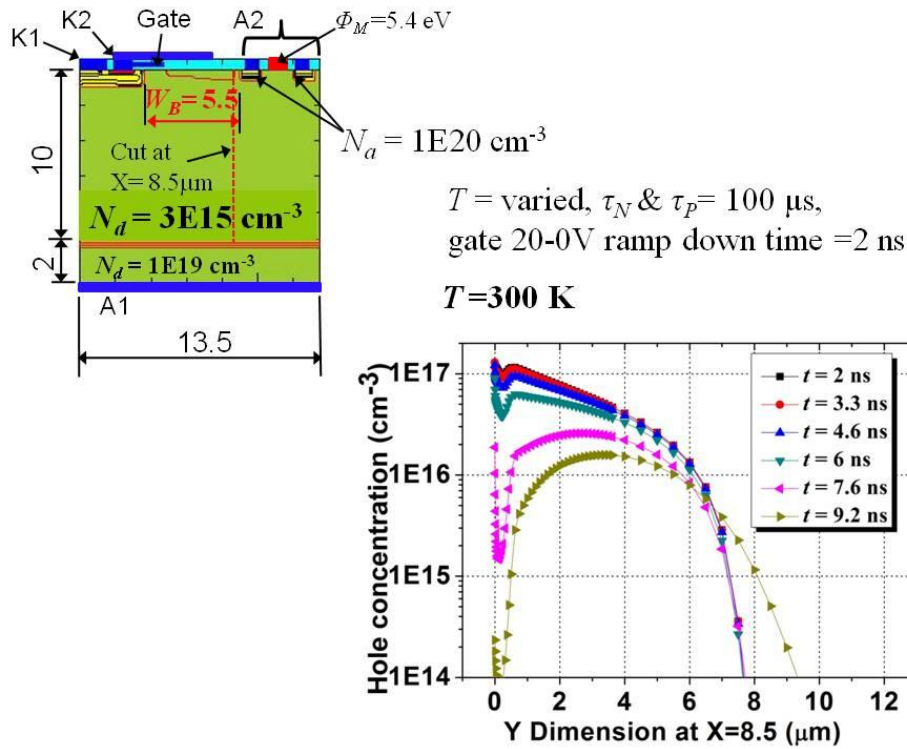


Figure 7.17. Decreasing hole concentration in lateral hybrid PNP base region (T_{R1}) or NPN collector (T_{R2}) during the switching event.

The lateral hybrid structure is very different to the other bipolar capable NPT IGBT due to in built resistive path to the anode 1 via the vertical resistance (R_V) as shown in figure 7.16, which allowed electrons to be extracted directly via the anode 1 terminal and via the Schottky to anode 2, thus limiting the concentration of holes in the PNP BJT base. As a result the concentration of holes in the PNP base region fell throughout the switching event of figure 7.12, as shown in figure 7.17.

During the self clamp operation of the lateral hybrid then the Schottky within the lateral hybrid (as described in chapter 6, figure 6.19) served to limit and reduce the carrier concentration within the PNP BJT base and hence V_{EB} of the PNP BJT was also limited. The charge storage as occurred in the IGBT meant that the V_{EB} of the PNP BJT within the NPT IGBT would continue to rise with $p_n=n_n$ in the conductivity modulated base region. In the lateral hybrid once the hole concentration (p_n) in the base region fell below $N_d = 3 \times 10^{15} \text{ cm}^{-3}$ then the PNP BJT base emitter junction was shown to have de-biased, hence the bipolar conduction stopped, reverting to unipolar conduction only. The action of the Schottky was therefore similar to previous works as reported by Shenai[18] and Krasnoperov[19] wherein a modified VDMOSFET with a lateral Schottky was demonstrated during unclamped inductive switching tests to improve the level of sustainable avalanche current capability over a standard VDMOSFET.

Once the base to emitter junction of the NPN BJT had de-biased ($V_{BE} < 0.7 \text{ V}$), both the electron and hole current fell rapidly to zero. Some hole storage in the PNP BJT base region occurred, but this charge was rapidly removed by the close proximity PNP BJT collector which was well within the minority carrier diffusion length (L_{pB}).

At $T=400 \text{ K}$, again conduction of the parasitic NPN was evident as anticipated, but as shown in figure 7.13 the resultant the turn off time to equilibrium was extended to 30 ns from 20 ns, as seen at $T=300 \text{ K}$. The extended period of conduction, from $t=8.75 \text{ ns}$ at $T=300 \text{ K}$ to $t=11 \text{ ns}$ at $T=400 \text{ K}$, enabled a greater duration of the self clamping effect which resulted in a reduced voltage peak developed across the reverse biased collector to base junction of the PNP BJT in the lateral hybrid of $V_1=27 \text{ V}$ as compared to $V_1=50 \text{ V}$ at $T=300 \text{ K}$. It must be noted however, that the energy available from the inductor was much lower at $T = 400 \text{ K}$, than at $T=300 \text{ K}$, as demonstrated by the voltage peak (V_1 , of figure 7.13) which was much lower than V_1 of figure 7.12. This was due to two factors: - firstly, as shown in table 7.2 the starting current at $V_{AK}=2 \text{ V}$ ($T=300 \text{ K}$) was $2 \times 10^{-4} \text{ A}/\mu\text{m}$, whereas at

$V_{AK}=1.6$ V ($T=400$ K) the starting current was reduced at $1.6E-4$ A/ μ m. In hindsight therefore, it would have been preferable to complete this test at the same starting current to enable a direct comparison as regards the voltage V_I achieved and the resultant conduction period. Secondly, the turn on of the parasitic NPN BJT at $T=400$ K occurred at a lower base to emitter voltage (V_{BE}) due to the reduction in V_{BI} and was conducting for a longer duration as the base emitter junction remained forward biased for longer.

7.5.4 Turn off energy comparison and effect on lattice temperature

The long duration of the resultant hole ‘tail’ current of the NPT IGBT, due to carrier storage and lengthy recombination period in the drift region as described by Baliga[6], caused a high turn–off energy (in units of joules) as represented by the area under the power density curve shown in figure 7.18. The similar procedure was completed on the VDMOSFET and lateral hybrid, a comparison of the turn off energy is summarised

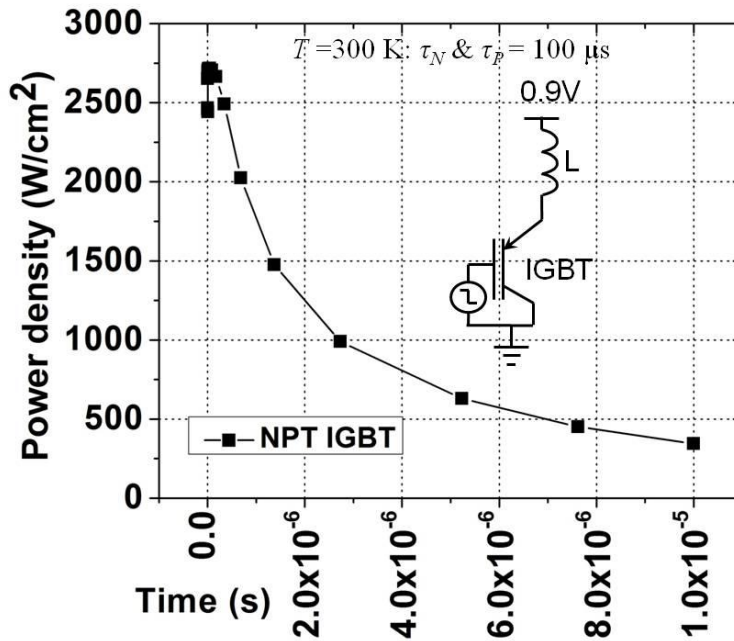


Figure 7.18. Power density developed within NPT IGBT as a result of unclamped inductive switching test.

against the IGBT in table 7.3. Clearly, the VDMOSFET displayed the lowest turn-off energy, whereas the NPT IGBT provided the largest turn off energy, but the lateral hybrid result was more similar to that of the VDMOSFET, than the IGBT. A comparison of the power density within the lateral hybrid during turn–off at $T=400$ K and $T=300$ K is shown

in figure 7.19. Clearly from figure 7.19 the largest turn off energy within the lateral hybrid occurred at the coldest temperature, however this result was also affected by the inequality of the inductor energy due to the difference in the initial current in the trials completed at $T=300$ K and $T=400$ K. The device physics with temperature however, dictate that the turn-off energy loss of the lateral hybrid would be increased at $T=233$ K due to the increase in V_{BI}

	VDMOSFET	IGBT	Hybrid
Turn-off energy (J/cm ²)	7.55×10^{-5}	8.72×10^{-3}	1.26×10^{-4}

Table 7.3. Comparison of turn –off energy at an ambient heat sink temperature of $T=300$ K.

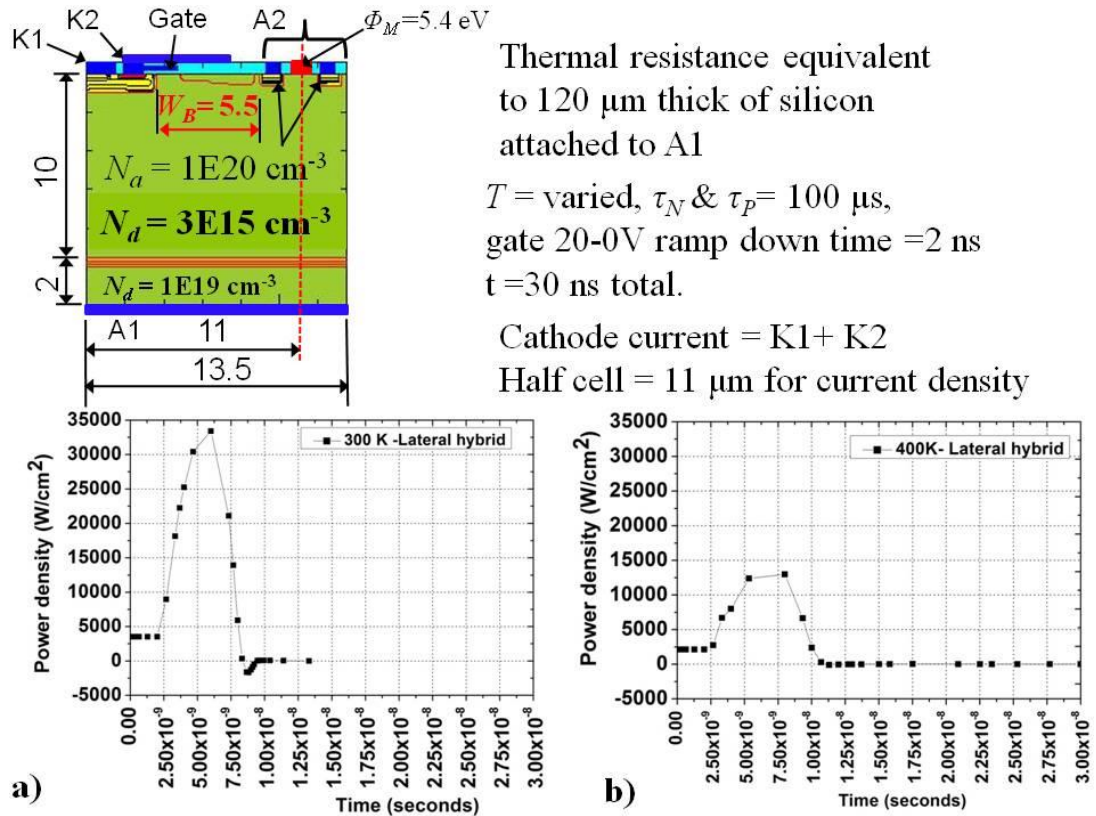


Figure 7.19. Comparison of power density with lateral hybrid during turn off transient at temperature of: - a) $T= 300$ K , b) $T=400$ K.

of the NPN BJT emitter to base junction and the reduced PNP BJT collector resistance. The cumulative effect of these factors would necessitate a higher hole current to activate the NPN BJT and the duration of conduction would be shortened as the hole current density in the collector would fall below that necessary to maintain V_{BE} in the NPN BJT more quickly

in terms of time (t). The voltage developed across the reverse biased junction therefore would be of higher magnitude, self clamping however, was still expected to occur in order to avoid avalanche, but this was not possible to be confirmed through simulation.

A direct comparison of the lattice temperature at $T=300$ K and $T=400$ K at various time intervals throughout the unclamped inductive switching event is shown in figure 7.20, clearly the reduced turn off energy at $T=400$ K enabled a reduction in the change of lattice temp between $t=2$ ns and the time at which the voltage V_1 was a maximum. In both cases the lattice temperature as recorded under the gate electrode demonstrated that the transient caused heating in the local channel area only which returned to that determined under initial conduction conditions at $t = 2$ ns as time approached that of the equilibrium condition. Once conduction ceased then at a rate determined by the substrate thermal impedance then the device would eventually return to the ambient heat sink temperature.

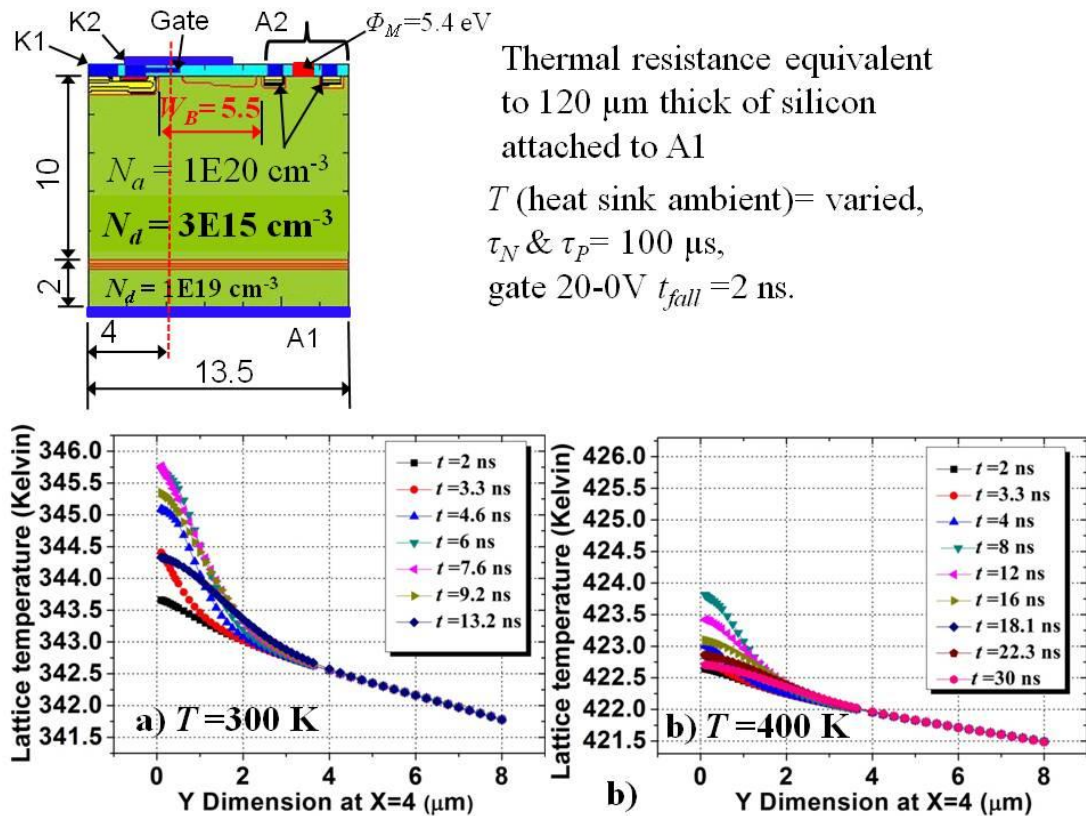


Figure 7.20. Comparison of instantaneous lattice temperature during turn off transient at ambient heat sink temperature of: - a) $T= 300$ K , b) $T=400$ K.

7.5.5 NPN-BJT activation.

The parasitic NPN BJT inherent within the P-body and MOS channel design within all of the compared structures is shown in figure 7.21. The method of activation of the NPN BJT is also shown in figure 7.21 via the Quasi Fermi Potential for holes (QFP) obtained from simulations of the lateral hybrid which equates to the base to emitter voltage (V_{BE}) of the NPN BJT, developed as the hole current was increased through the P-body throughout the duration of the UIS switching event as shown in figure 7.22. The QFP plots can be directly compared at any time (t) during the UIS transient to the plots of hole current density

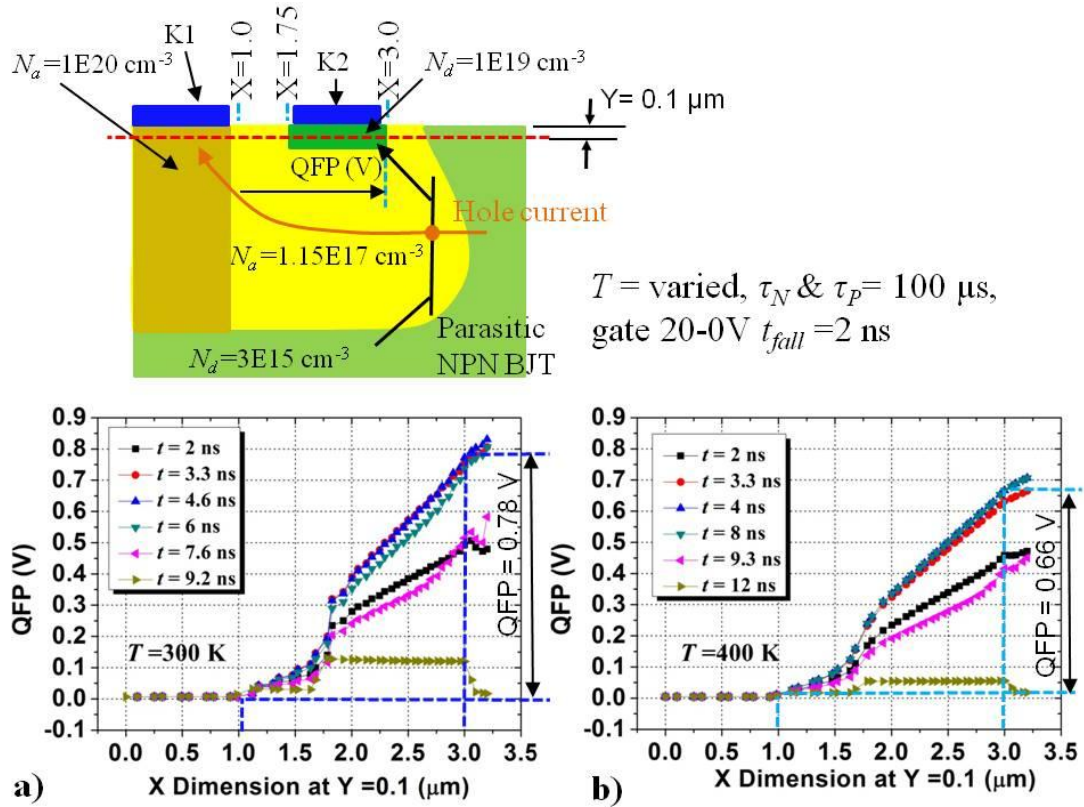


Figure 7.21. Comparison of Quasi Fermi Potential for holes (QFP) during turn off transient at temperatures of : a) $T=300 \text{ K}$, b) $T=400 \text{ K}$.

within the P-body, or collector of the PNP BJT, (again at $T=300 \text{ K}$ and $T=400 \text{ K}$) as shown in figure 7.22. The comparison demonstrated the effect of junction temperature on the PNP BJT collector resistance and the V_{BI} of the NPN BJT base to emitter junction at $T=400 \text{ K}$. As can be seen activation of the NPN BJT occurred at a lower current density at $T=400 \text{ K}$ compared to that at $T=300 \text{ K}$ due to the reduction in V_{BI} of the base to emitter junction of the

NPN BJT and increase in resistance of the PNP BJT collector. This in turn was due to the change in Fermi level as a subsequence of the increase in temperature and concentration (Grove[7]).

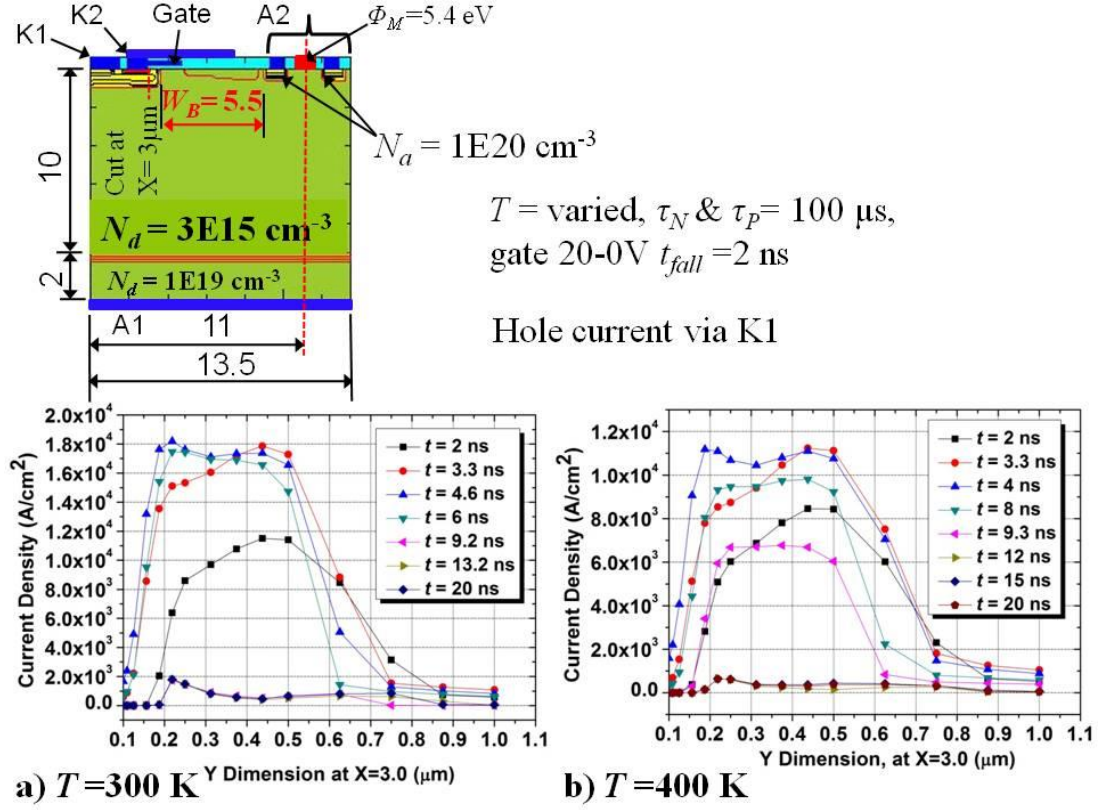


Figure 7.22. Comparison of power density with lateral hybrid during turn off transient at temperature of: - a) $T = 300 \text{ K}$, b) $T = 400 \text{ K}$.

As can be seen through the direct comparison of current density with QFP then as the hole current density falls as time (t) increments then QFP also falls simultaneously. Eventually the NPN BJT de-biases and ceases conduction at $t = 7.6 \text{ ns}$ in the case of $T=300 \text{ K}$ and at $t = 9.3 \text{ ns}$ at $T=400 \text{ K}$. The conduction of the NPN BJT is thus totally dependent upon the hole current.

The activation of the parasitic NPN BJT within a VDMOSFET was evaluated and discussed by Fischer[20] during UIS trials; this resulted again in non sustained activation of the NPN BJT. In the case of the lateral hybrid as the conduction of the NPN BJT was not sustained, as described in the preceding sections the NPN BJT activation was actually desirable to prevent avalanche of the lateral hybrid device and prevent the associated slow

recovery time and increased energy loss. In the NPT IGBT the identical P-body and channel design meant that it too was susceptible to latch up, but at the initial current of $I_K = 1.5E-4$ A/ μm at $V_{AK} = 0.9$ V, (at $T = 300$ K) the inductive energy was not sufficient to cause activation of the NPN BJT as most of the hole current by passed the N+ cathode diffusion by travelling in a vertical direction from the P+ Anode to the cathode via the P-body to cathode short where $N_a = 1E20 \text{ cm}^{-3}$, as shown in figure 7.21, as this formed the lowest resistance path. Whereas with sufficient hole current passing under the N+ cathode in the IGBT, the activated parasitic NPN, would form a Thyristor structure as shown in figure 7.23. When the NPN BJT side was activated then electrons would flood into the lightly doped regions

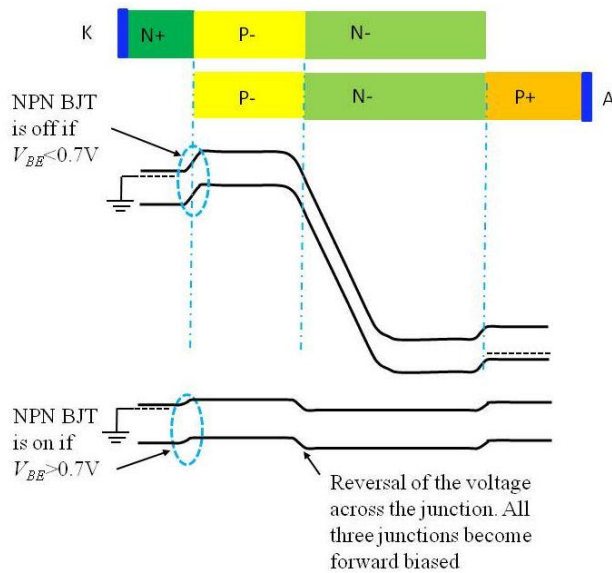


Figure 7.23. A generic thyristor structure and band diagrams in the off and on state.

simultaneously enabling additional holes to flood in from the P+ region, thereafter the device conducts like a PiN diode according to Sze[4], where the 'i' region becomes conductivity modulated allowing electrons to recombine in the P+ region and holes in the N+ region, leading to current at the terminals.

7.5.6 Comparison of electro-mechanical to semiconductor switching.

From review of the EV200 series datasheet from Tyco[1] a number of switching issues were evident. These issues included intolerance to repetitive fault current switching and the need

to pre-charge capacitors to prevent surge current and hence possible arcing damage to the contacts (as described in chapter 2, figure 2.2) even though arc suppression techniques and vacuum switching were utilised. The contacts also suffered from contact bounce and an extended time of contact actuation, therefore switching times were extended to 12 ms in comparison to <20 ns to $10\text{ }\mu\text{s}$ for the compared semiconductor devices. Most importantly a situation equivalent to latch up of an IGBT could potentially occur if the contacts welded shut during fault current switching.

In the inductive switching tests completed on the compared semiconductor devices then the VDMOSFET provided the shortest switching time closely followed by the lateral hybrid, however in the SSPC application switching time was not a major consideration other than to reduce the turn off energy and hence reduce the dynamic loss. Provided the semiconductor lattice temperature at $T=400$ K during the switch transient could be maintained below the manufacturer's upper operating limit ($175\text{ }^{\circ}\text{C}$ max) then repetitive switching events could occur without degradation. In contrast the CB had a fixed life span of one million operations provided that it was operated within the specifications and design guidelines, but as discussed in chapter 2, figure 2.2, the contact life was rapidly degraded by surge current events and ended after a single fault current event.

7.6 Electro-mechanical switch replacement

Having compared the possible replacement semiconductor structures in both static and dynamic tests it was now possible to select which of the possible replacement devices may best suit the MEA application as described in chapter 2 and summarised in the mission profile of section 7.2. The resultant active device was ideally also to have a minimised silicon area, but performance, reliability and ruggedness were the key criterion. Switching time was neglected as a direct measure, but was factored into the dynamic losses. A summary is shown at table 7.4 which compares the electro-mechanical contactor to the compared structures of figure 7.1 and a modular construction consisting of a VDMOSFET and NPT IGBT.

The EV200 electro-mechanical switch was given 10 out of a possible total of 40 for its low on state static and dynamic switching, but this was dependent upon adherence to the specification and design guidelines provided by the manufacturer. The predominant failure of the EV200 is caused by arcing which becomes detrimental to life expectancy in the event

Parameter	EV200	VDMOSFET	IGBT	Hybrid	Modular MOSFET/IGBT
Life	1million, but degraded with fault current	>1 million	>1 million	>1 million	>1 million
Power loss: static	Lowest	Low $V_{AK}<0.7V$	Very Low $V_{AK}>0.7V$	Less than MOSFET at $V_{AK}<0.7$ Lower than MOSFET, but higher than IGBT at $V_{AK}>0.7V$	Nominal current: as VDMOSFET Fault current: as IGBT. Requires device matching and careful gate interconnect layout
Power loss: dynamic	Lowest at nominal current. Results in arcing damage particularly at fault current	Lowest: latch up free, but may avalanche with large inductive load	Highest: susceptible to latch up	Medium: latch up free, self clamping. Large inductance load capable	Nominal current: as VDMOSFET Fault current: as IGBT. Requires optimised gating between classes of device
Operating temp (°C)	-40 to +85	-40 to +127	-40 to +127	-40 to +127	-40 to +127
MEA Score	10	30	30	35	35 (if matched & optimised)

Table 7.4. Switching element comparison for MEA application in power distribution.

of high current transients. The reliability of the CB device is therefore compromised. If the replacement switching element was chosen to be the modular MOSFET/IGBT then in theory this should give the lowest static loss under most conduction conditions, all except the high turn off or dynamic loss of the IGBT. Unfortunately, practical considerations prevent this solution from becoming realised on a volume production basis due to the mismatch between devices and the gating of those. If the IGBT type were used alone then again the high dynamic loss and no current control below $V_{AK}\approx 0.8V$ would be negative factors. This leaves the VDMOSFET with increased active area, or the lateral hybrid as options. The

VDMOSFET option could possibly enter avalanche during switching of the inductive load and hence thermally expire due to the associated high losses due to the energy of the simultaneous high current and voltage. The lateral hybrid however, provided a self clamping mechanism and therefore either the current through the inductive load could be much larger than that of the VDMOSFET, or the inductive load could be much larger. Either way the lateral hybrid would prove to be a much more rugged switching element, particularly in a fault current event. In the event that avalanche did occur in the lateral hybrid (which is most likely at $T=233$ K) then the Schottky would enable a faster recovery than that of the VDMOSFET.

7.7 Summary

A summary of the compared attributes of the VDMOSFET, NPT IGBT and lateral hybrid are shown in tables 7.5 and 7.6. In relation to the mission profile of section 7.2 a comparison of each power switching device investigated was made against a modular MOSFET/IGBT connected in parallel and a typical electro-mechanical contactor. A lateral hybrid was chosen due to the ability to self clamp, thus increasing the current level required to any given inductive load in order to cause avalanche. The lateral hybrid was selected as it was potentially more rugged than a large area VDMOSFET, this was the primary requirement of the switching element to be used with the More Electric Aircraft (MEA).

Attribute number	Attribute description	VDMOSFET	NPT IGBT	Lateral hybrid
1	Reverse leakage level increase with ambient heat sink temperature	Lowest leakage level rise: $1\text{E-}11$ A/ μm at $T=400$ K $2\text{E-}14$ A/ μm at $T=300$ K: rise = 3 orders of magnitude	Highest leakage level rise: $1\text{E-}9$ A/ μm at $T=400$ K $4\text{E-}14$ A/ μm at $T=300$ K: rise = 5 orders of magnitude	similar to VDMOSFET: $2\text{E-}11$ A/ μm at $T=400$ K $3\text{E-}14$ A/ μm at $T=300$ K: rise = 3 orders of magnitude
2	Forward BV	Lowest reduction with increasing ambient heat sink temperature $BV=87$ V at $T=300$ K , $BV=85$ V at $T=400$ K	Highest reduction with increasing ambient heat sink temperature $BV=84$ V at $T=300$ K , $BV=50$ V at $T=400$ K Reduction due to open base transistor breakdown	More similar to reduction in VDMOSFET with increasing ambient heat sink temperature $BV=84$ V at $T=300$ K , $BV=76$ V at $T=400$ K Reduction due to open base transistor breakdown
3	Reverse BV	No: Body diode conducts	Symmetrical with forward BV	No: Body diode conducts
4	Self heating temperature coefficient at $T=300$ K, $V_{GK}=20$ V	Positive TCR: die can be used in parallel Linear region: $dI/dV = 2.5\text{E-}4/0.8$ ((A/ μm)/V) Saturation region: lowest current increase for highest voltage increase: $dI/dV = 0.25\text{E-}4/1.5$ ((A/ μm)/V)	Positive TCR: die can be used in parallel Bipolar region: highest current increase for lowest voltage increase: $dI/dV = 2\text{E-}4/0.3$ ((A/ μm)/V)	Positive TCR: die can be used in parallel Unipolar linear region: $dI/dV = 2.5\text{E-}4/0.8$ ((A/ μm)/V) Bipolar region: $dI/dV = 1.5\text{E-}4/0.5$ ((A/ μm)/V)
5	Bipolar start up voltage (V_i)	Unipolar conduction only: No bipolar mode except in reverse conduction via body diode (PiN type)	No unipolar conduction: (therefore fixed forward volt drop) Bipolar conduction starts at: $T=400$ K, $V_i = 0.5$ V $T=300$ K, $V_i = 0.70$ V $T=233$ K, $V_i = 0.8$ V Range = 0.3V : $T=400$ K to $T=233$ K	Unipolar conduction as per VDMOSFET Bipolar conduction starts at :- $T=400$ K, $V_i = 1.05$ V $T=300$ K, $V_i = 1.65$ V $T=233$ K, $V_i = 2.15$ V Range = 1.1V $T=400$ K to $T=233$ K Bipolar mode also available in reverse conduction via body diode (PiN type)
6	Unclamped Inductive Switching ($T=300$ K) $L=0.9$ mH	Switch off time to equilibrium = 20 ns (if not entered avalanche). Lowest switching energy if avalanche does not occur.	Longest switch off time to equilibrium = $10\mu\text{s}$, highest switching energy due to long recovery to equilibrium	Same switch off time to equilibrium as VDMOSFET (20ns). Switching energy level closer to VDMOSFET. More than an order of magnitude less than IGBT
7	Activation of parasitic NPN BJT	Possible in the case of avalanche- non sustained.	Activation possible at high current, relatively low current activation also possible without the now standard P-body and N+ emitter design improvements. Causes 'latch up' of device in thyristor type manner- loss of gate control	Liable, but conduction of NPN BJT is not sustained. Activation necessary to perform self clamped inductive switching.
8	Self clamping or external clamp required?	External clamp required	External clamp required	Self clamping, high inductance load capable, rugged.

Table 7.5. Comparison of Attributes discussed of the structures of figure 7.1

Attribute number	Attribute description	VDMOSFET	NPT IGBT	Lateral hybrid
9	$R_{(ON,SP)}$ $T=300\text{ K}$, $V_{GK}=20\text{ V}$, $V_{AK}=0.9\text{ V}$	1.90 mΩcm ²	0.334 mΩcm ²	3.11 mΩcm ²
10	$R_{(ON,SP)}$ $T=300\text{ K}$, $V_{GK}=20\text{ V}$, $V_{AK}=2\text{ V}$	2.25 mΩcm ²	Not Applicable	1.16 mΩcm ²
11	Area for 100A? $T=300\text{ K}$, $V_{GK}=20\text{ V}$, $V_{AK}=0.9\text{ V}$	0.212 cm ²	0.0372 cm ²	0.345 cm ²
12	Area for 100 A? $T=300\text{ K}$, $V_{GK}=20\text{ V}$, $V_{AK}=2\text{ V}$	0.113 cm ²	Not Applicable	0.0579 cm ²
13	Area for 1000 A? $T=300\text{ K}$, $V_{GK}=20\text{ V}$, $V_{AK}=2\text{ V}$	1.13 cm ²	Not Applicable	0.579 cm ²

Table 7.6. Comparison of $R_{(ON,SP)}$ and Area

7.8 References

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Chapter 8 | Conclusions and recommendations

8.0 Introduction

This final chapter presents the conclusions of the research work completed. The potential impact of this work is summarised on the future solid state power controller (SSPC) designs. A recommendations section is also provided in which the valid further work necessary in order to maximise the benefits of the power semiconductor device structure are described.

8.1 Conclusions

Driven by the global need to reduce CO₂ emissions, the aim of the More Electric Aircraft (MEA) is to reduce the weight and hence improve the fuel efficiency of the aircraft and yet improve, or at least maintain, the reliability of the present aircraft. The main body of this research work was to create and evaluate a new rugged semiconductor power switching device structure for use within an SSPC for the MEA, ultimately replacing the existing electro-mechanical contactor within the power controller.

Power semiconductor switching devices for the SSPC are required to demonstrate lowest loss under all conditions, both static and dynamic, hence reducing wasted energy in the form of heat, thus reducing the risk of catastrophic device failure due to the effects of self generated heat. For a possible semiconductor replacement in low to medium power applications ($BV=100$ to $1200V$, current = 10 to $1000A$) the MOS type devices with their

voltage controlled gate were considered most appropriate due to the minimised gate drive requirements. The limitations of traditional MOS devices such as the IGBT and VDMOSFET are well known in terms of static and dynamic losses. The unipolar VDMOSFET provided lowest dynamic loss and low static loss in the linear region of operation, but in an over current situation the VDMOSFET device could saturate if the active area was not large enough, potentially suffering avalanche and thermal failure as a direct result. The IGBT had a large dynamic loss, but benefitted from the lowest static loss and lowest active device area. Unfortunately, a fixed forward volt drop within the IGBT was also incurred prior to bipolar conduction whereas the VDMOSFET could conduct from $V_{AK} = 0.1 \text{ V}$ rather than $V_{AK} \approx 0.8 \text{ V}$.

To overcome these limitations one method to obtain lowest conduction loss under all conditions was to use a modular construction of both VDMOSFET and IGBT device classes operating in parallel. The difficulty however, was the need to use matched devices and complex gating arrangements to ensure balanced current flow in each IGBT die under fault conditions. Within the modular solution however, the high dynamic loss of the IGBT unfortunately remained an issue as concerned reliability. This was due to thermal effects and the increased risk of latch up at high temperatures when turning off any fault current through an inductive load. A hybrid device to combine the benefits of the unipolar and bipolar conduction was therefore required.

The concept of a new class of hybrid device for the SSPC was validated at $BV \approx 100 \text{ V}$ and is based on a MOS gated VDMOSFET designed for lowest on state loss as optimised using Taguchi statistical methods to good effect as demonstrated within chapter 3. This utilised a DMOS P-body structure as literature review revealed that this structure to be more rugged than the higher current density UMOS or trench gate. An $R_{(ON,SP)}$ of $3.1 \text{ m}\Omega\text{cm}^2$ at $V_{AK} = 2 \text{ V}$, $V_{GK} = 17 \text{ V}$ with $BV = 124 \text{ V}$ was achieved which was very close to the 1-D silicon limit with low threshold voltage ($V_{TH} = 5.5 \text{ V}$ at $T = 300 \text{ K}$) and high transconductance (g_{mL}) and high saturation current level ($I_{A,sat}$).

In order to achieve conductivity modulation and bipolar conduction within the unipolar VDMOSFET then an injector structure was required to operate in conjunction with the P-body also functioning as a collector of the injected minority carriers. The injector structure therefore enabled operation of a parallel bipolar conduction path in addition to the unipolar conduction. As described in chapter 4 the novel injector structure was formed using a merged high barrier height ($\Phi_M=5.4$ eV) Schottky and acceptor doped anode (similar to a JBS, Junction Bipolar Schottky diode anode), placed either vertically (on the bottom of the wafer) or laterally (adjacent to the channel region). The novel merged Schottky P-Anode injector provided the following functions:-

- a) High level injection was achieved in the N-Drift region.
- b) Bipolar conduction was provided via an integral PNP BJT in parallel with the unipolar conduction path.
- c) Dependent upon the placement of the injector (either vertical or lateral), the emitter to base bias (V_{EB}) of the PNP BJT in bipolar mode was controlled by the Schottky which in turn controlled $I_{A,sat}$ and also V_i in the vertical structure.
- d) Schottky barrier height (Φ_{Bn}) could also be used to adjust the saturation current ($I_{A,sat}$) in bipolar mode. A high barrier height was required to ensure highest level of conductivity modulation and $I_{A,sat}$, thus requiring a high metal work function contact (PtSi, where $\Phi_M=5.4$ eV).
- e) The Schottky enabled increased PNP BJT current gain (α) through hole storage in N-Drift region.

The benefits of using the novel injector structure were reviewed in chapters 5 and 6 as compared within a vertical and laterally injected VDMOSFET structure. A direct comparison of these structures can be seen in table 6.6. To minimise dynamic losses any hybrid device would be used in unipolar mode at nominal current levels, but operate in bipolar mode during fault conditions only as achieved through a self biased transition. The benefit of the lateral hybrid over the vertical injected structure was that it provided lowest

$R_{(ON)}$ in unipolar mode and yet in bipolar (or fault current) mode it could also be optimised to demonstrate an improved bipolar performance in comparison to the vertical hybrid. The limitations of the BV could be overcome, in the lateral hybrid, through the use of commercial processes to create a charge balance structure. The only optimisation possible to improve the unipolar performance on the vertical hybrid was to minimise the active area of injected cells to non injected cells, hence reduce $R_{(ON)}$ in unipolar mode. The impact of which may be to cause reduced reliability due to hot spots during fault conditions through high current density in the gate regions directly above the injector.

Through direct comparison of the created lateral hybrid with a standard VDMOSFET and NPT IGBT, of identical rating ($BV \approx 84$ V), the static and dynamic losses were evaluated and compared. The static conduction losses were verified at three ambient heat sink temperatures $T = 233, 300$ and 400 K. While the comparison of the dynamic performance, when switching an unclamped inductive load, was evaluated at $T = 300$ and 400 K. Where possible these tests were completed at a start current magnitude which was in the bipolar part of the I-V characteristic, the results are summarised in tables 7.5 and 7.6.

Importantly the lateral hybrid incorporating the novel merged Schottky P-Anode demonstrated through the dynamic testing that the parasitic NPN BJT which caused latch up in IGBT type devices was activated, but in the case of the lateral hybrid conduction was not sustained. Indeed the NPN BJT conduction allowed the lateral hybrid to self clamp. The self clamping enabled a higher current switching through a given inductance load without incurring avalanche and the associated long recovery to equilibrium and/or potential thermal failure.

Despite an increased load current the lateral hybrid in bipolar mode switched almost as quickly as the compared unipolar VDMOSFET. Dynamic loss (or turn off energy, E_{off}) in the lateral hybrid therefore was reduced in comparison to the IGBT due to the limited V_{EB} as enabled by the Schottky contact within the novel merged laterally placed anode. The turn off

energy (E_{off}) within the lateral hybrid also reduced as ambient heat sink temperature (T) increased.

The lateral hybrid therefore achieved increased ruggedness as compared to the modular construction solution (of IGBT and MOSFET die) due to the high dynamic losses of the IGBT class of device. In addition the single gate control of the lateral hybrid also enabled ease of manufacturing and lower potential unit cost as it removed the need to use matched device die, the need for complex gate timing, or require matched conductor parasitic elements to each die to ensure that no single die conducted more current at any time than any other in order to reduce the risk of cascade die failure. The active area of the lateral hybrid however, would be higher in unipolar mode than using VDMOSFET die alone, however if the VDMOSFET and lateral hybrid were sized to conduct the fault current then the required hybrid area would be lower by a factor of approximately one half, as shown in table 7.6.

The lateral hybrid design, incorporating the novel merged injector, when sized correctly for the expected fault current, therefore was expected to be extremely rugged in the SSPC application within the MEA during fault current switching due to the ability to safely maintain the fault current conduction until the sensor and control system could gate off the device, the low static loss in unipolar mode (area dependant) and reduced energy turn-off when in bipolar mode in comparison to the IGBT would thus allow a safe and reliable shut down via a single gate control. Such a safe and controlled shutdown could be repeatable many times as the semiconductor had no mechanical parts to wear or contacts to arc unlike the electro-mechanical contactor.

8.2 Recommendations

The main issue with the lateral hybrid concept as presented herein was the blocking voltage (BV) upper limit as caused by the exposed radius of curvature and the need to minimise the base width (W_B) in order to reduce the bipolar start up voltage (V_i). The minimised W_B adversely affected the open base transistor breakdown (BV_{CEO}). In order to achieve a device rated $BV=500$ V for the MEA SSPC then future work could be directed towards amendment of the concept design to enable the incorporation of charge balance techniques. Relevant works which indicate that this method would provide an increased BV rating in the lateral hybrid are by Appels[1] as regards the lateral RESURF technique and for the vertical charge balance the work of Fujihira[2, 3] and Deboy[4]. The proposed full cell structure is shown in figure 8.1.

Although the fundamental operational principles of the lateral hybrid design are similar, the optimisation of both geometry and doping within the proposed charge balance structure is very different to that of the concept lateral hybrid device and requires further work to be understood fully and optimised accordingly. It is estimated that the now vertical base width (W_B) of the PNP BJT would be much reduced and would therefore provide a means of increased PNP BJT gain, reduced bipolar start up voltage (V_i) and hence provide a reduced on state loss in bipolar mode. This would enable an active area reduction for a given fault current level. The on state loss in unipolar mode would also be decreased in line with standard vertical charge balance MOSFET designs which allow the use of increased N type doping in the N-Drift region and hence reduced $R_{(ON,SP)}$ and yet boosted BV to the target of 500 V. due to the lateral element to the electric field profile. The maximum depletion width extending from the P- lateral charge balance element into the PNP BJT base region could be controlled with locally increased n-type doping to obtain a $V_{PT} \geq BV$.

The concept hybrid design can provide a rugged, fault tolerant, unipolar-bipolar hybrid at a $BV \approx 100V$, which can satisfy a large number of safety critical automotive type

applications (where operating voltage = 48V max). In this instance further work is required firstly to verify the simulations via actual fabrication and test of the proposed device. If fabricated then key questions could be answered such as for a given active area what would be maximum rated fault current under static conditions? Furthermore under dynamic conditions how many such fault current switch off incidents could be safely endured and are there any quantifiable measures which could be continuously monitored to enable a prediction of future failure? Variation from a strictly 1:1 ratio of injected VDMOSFET cells to non injected VDMOSFET cells in a given active area could also be investigated. Finally, the effect on the static and dynamic characteristics of the proposed lateral hybrid to an

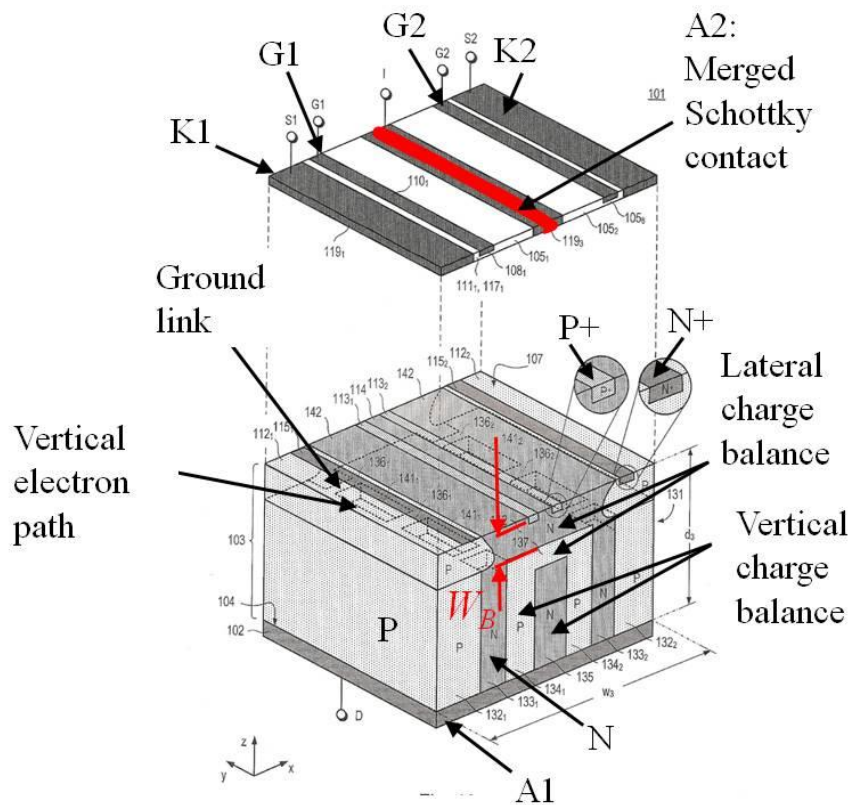


Figure 8.1. Proposed structure of a charge balanced variant of the lateral hybrid.

ambient heat sink temperature of $T=233$ K also required to be established using fabricated and packaged devices to firmly establish performance. Under fault conditions at $T=233$ K however, the resultant rapid warming of the lattice may prevent the need for any lateral hybrid device Safe Operating Area de-rating as the device physics (V_{BI} reduction of the P-

Anode to N-Drift junction with increased lattice temperature), due to self heating, act so as to enable reduction of the device losses in bipolar mode.

Additional work is required to make a device comparison between a silicon hybrid (without charge balance) and one using silicon carbide. The use of silicon carbide (with a high dielectric constant) would enable a much reduced drift length to around 4 μm providing $BV \approx 1$ kV. The work is required to determine the minimum base width of the internal lateral PNP and what effect the Schottky metal work function has on the resultant bipolar start up voltage (V_i).

For both silicon and silicon carbide lateral hybrid device types then another area of future study would be to optimise the relative areas of the P-Anode to Schottky in the merged injector contact to understand the effect of area and possibly the shape of the injector. This study would require a full 3-D simulation and /or fabrication.

8.3 References

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Appendix 1 | Published paper

A1.0 Introduction

This appendix contains the published paper from the work contained within chapter 7 of this thesis. The paper was presented at EPE2011 conference in Birmingham, U.K.

Introduction of a hybrid MOSFET-IGBT power switching device utilising a novel Schottky biased minority carrier injector

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Acknowledgements

This work has been supported by the EPSRC in the U.K. The Authors thank Mark Johnson, Jon Clare of the University of Nottingham, Tony Lakin of Turbo power systems Ltd, Adrian Shipley and Mark Harrington of G.E Aviation Ltd all for their support and feedback throughout the project.

Keywords

«Minority carrier injector», «Insulated gate bipolar transistors», «Fault tolerance», «Power MOSFET»,

Abstract

A new minority carrier injector is described and demonstrated via simulation within an otherwise standard Vertical Diffused Metal Oxide Semiconductor Field Effect Transistor (VDMOSFET) structure forming an injected hybrid device. The resultant hybrid structure is directly compared to a standard Insulated Gate Bipolar Transistor (IGBT) and unipolar VDMOSFET of identical Blocking Voltage (BV). The hybrid is shown to be a latch up free device which switches an inductive load within a comparable time frame to a unipolar MOSFET, and yet at an ambient heat-sink temperature of 300 Kelvin the bipolar hybrid achieved double the current density of the unipolar MOSFET at Gate to Cathode voltage (V_{GK})=20 V, Anode to Cathode voltage (V_{AK})=2 V. At 400 Kelvin, V_{GK} =20 V, V_{AK} =1.65 V the specific on state resistance (RAK_{ONSP}) of the hybrid was found to be $1.14 \text{ m}\Omega\text{cm}^2$ as compared to $3.26 \text{ m}\Omega\text{cm}^2$ of the unipolar MOSFET. The net effect of this hybrid device is to provide lowest on state loss MOSFET type performance from V_{AK} =0.1 V with built-in, self biased, bipolar protection in the event of surge current. Any increase in junction temperature as a result of surge current or over voltage only serves to assist the onset of the low loss bipolar mode. The concept is to target the 600 V market.

Introduction

This paper describes the design and benefits of a new Schottky biased minority carrier injector. This injector can be incorporated into either silicon or silicon carbide MOS (Metal Oxide Semiconductor) device topologies in order to reduce the on state loss at a given Blocking Voltage (BV). An example usage of such an injector within a Silicon VDMOSFET (Vertical Double diffused Metal Oxide Semiconductor Field Effect Transistor) is described herein. The performance of this example device is directly compared to that of a standard (non injected) VDMOSFET and IGBT (Insulated Gate Bipolar Transistor) of identical BV at an ambient heat sink temperature of 300 Kelvin (K).

Although the resultant cell area of the injected VDMOSFET (named the ‘hybrid’) is double that of the non injected VDMOSFET, the hybrid can safely conduct, and quickly switch off (<30 ns), double the current density at the identical Anode Cathode Voltage (V_{AK}) and Gate Cathode Voltage (V_{GK}). In comparison the example IGBT device can conduct high current with a lower forward volt drop (V_{AK}) than the hybrid, but will not begin conduction until $V_{AK} > 0.7$ V, in addition the switch ‘off’ time is very long (>10 μ s) which restricts the switching frequency of such a device. A VDMOSFET however, is simply a resistor in the linear region, but will enter a high resistance (saturated) state in the event of an over current or over voltage event, thus the active area required to conduct a known current within the linear region is key to reliable operation. The advantage of the MOSFET is the high speed switching (turn-off <30 ns), indeed, a charge balanced MOSFET can switch too quickly causing high dynamic losses. Thus essentially the main commercially available power devices have very different strengths and weaknesses and hence are used in different applications, placing different constraints on the system design. In pursuit of lowest on state loss in the BV region of ≤ 600 V, charge balanced silicon MOSFET structures DeBoy[1] have tended to dominate in the absence of successful wide band gap MOSFETs. Similarly, at 600 V to 1200 V, silicon Trench Field Stop IGBTs, Laska[2] dominate. Other approaches include the new reverse conducting IGBT devices, Rahimo[3] as researchers and manufacturers attempt to improve the range of suitable applications for the silicon devices available as regards on state loss, blocking voltage and switching speed.

The Schottky biased minority carrier injector proposed here however, will enable a new class of hybrid devices which combine the benefits of lowest on state loss (from $V_{AK} = 0.1$ V) and fast, latch-up free, switch ‘off’ (<30 ns) which could be applied to both charge balanced MOS or silicon carbide (SiC) simple DMOS.

Power switching state of the art

Ideally a power device would switch instantly via an infinite resistance voltage control, have no leakage current to infinite forward or reverse voltage when gated ‘off’, and zero ohm resistance when ‘on’ with no saturation limit which would otherwise lead to a high resistance state. As the ideal does not exist then a practical way of achieving an improved balance between the commercially available VDMOSFET and IGBT is to use them in parallel in order to switch high currents as shown in figure 1a with the resultant hybrid characteristic shown in figure 1b. Work has been completed on such parallel MOSFET-IGBT structures using discrete devices, for example by Kimball[4], Kaerst[5] and Hoffmann[6]. The resultant modular device structure

offers lowest on state loss at all times, while the IGBT also offers surge current protection to the MOSFET. Indeed, a MOSFET is particularly susceptible to over current damage as demonstrated by the work of Lefebvre[7] which compared the limited robustness to short circuit energies of charge balanced MOSFET devices and Insulated Gate Bipolar Transistors (IGBT). The difficulty however, is that all the devices not only need to be matched for Blocking Voltage, but also gate threshold voltage (V_{TH}) as a minimum, there is also a myriad of parameters that need to be considered when operating at a high switching frequency or with expected transients (in terms of voltage and/or current). If the devices are not carefully matched (including the parasitic circuit elements leading to each die) then it is possible for one device to begin conducting earlier than the others, hence it may fail causing a cascade of failure in the remaining devices through over current. The optimisation of the gate signal timing is also critical to the success of a modular power switch as per the work of Yee[8]. An alternative to using matched devices is to independently control the voltage across each die, (hence control the current) as described by Palmer[9]. Independent control however, adds complexity (reduced reliability) and cost to any system.

One potential solution to the issues described above is to fabricate the MOSFET and IGBT on the same die to form a hybrid. The resultant high current density die has only the variation that exists across its active area. The reliable conduction of high transient current is no longer dependent upon the wider tolerance limits of wafer to wafer or batch to batch fabrication as with the use of discrete commercial die. In order for a unipolar MOSFET structure to enter a low loss conduction state (below the silicon limit) then a minority carrier injector is required as targeted by the work of Chow[10] and Liu[11, 12]. These researchers both tried to utilise a lateral injector. However, to date, all previous attempts had either failed to demonstrate significant levels of injection and/or required additional external biasing so were not suitable for hybrid device commercialisation.

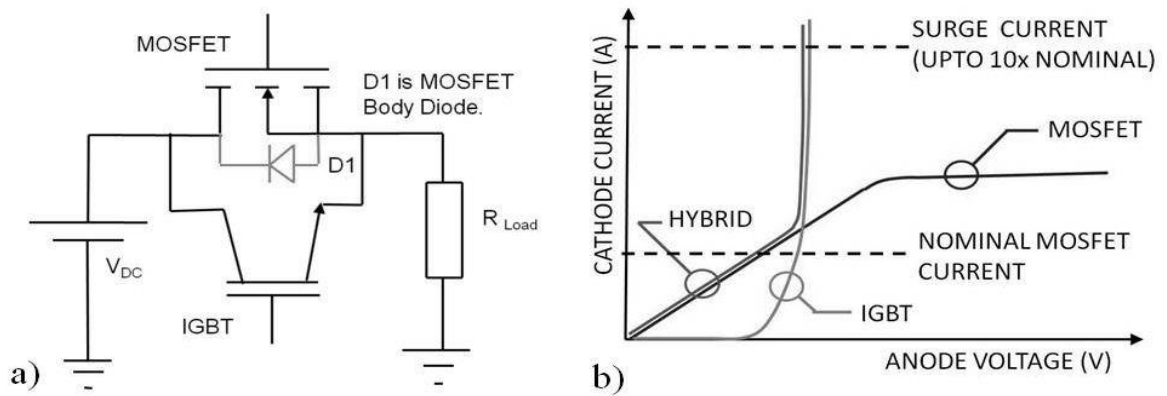


Fig. 1: a) Parallel use of MOSFET and IGBT to control load current. b) A hybrid demonstrates reduced on state loss throughout the characterised range while the MOSFET and IGBT both demonstrate a high loss region at either high or low Anode Voltage respectively.

In contrast to the laterally injected hybrid die there is a vertically injected option developed recently by Rahimo[3] in which hybrid MOSFET-IGBT operation is also feasible, called the Reverse Conducting IGBT (RC-IGBT) or BIGT (Bi-mode Integrated Gate Transistor) concept. The aim of the RC-IGBT type is to incorporate a body diode operation into an IGBT structure in order to improve inductive load switching performance of the IGBT in terms of switching speed and enable load clamp diode removal. This was accomplished by

adding Anode (collector) N type shorts through the P+ implanted injector on the back side of the thinned wafer, once the top side has been patterned to form the multiple MOS channel regions. This device required no external biasing and remained a three terminal device. The logical extension of this development is that electron flow (MOSFET conduction) via the Anode (collector) is now possible, but the start up of minority carrier injection is now totally dependent upon the resistive voltage drop developed across the p-type injector by the electrons as they traverse to the Anode. The problem with the resistive biasing of the backside wafer injector is that ‘snap back’ occurs when transitioning from the unipolar conduction to bipolar conduction mode. This is particularly a problem for the backside injector at ambient heat-sink temperatures ≤ 350 K. The RC-IGBT type structure has the potential for injection start up (in terms of V_{AK}) to be potentially as low as an IGBT, however, this requires a greater P injector (IGBT collector) width relative to the N type width (MOSFET drain). Increased P type width on the Anode relative to N type width reduces the MOSFET conductance, hence requires a much greater area in order to obtain a low Anode to Cathode resistance (R_{AKon}) MOSFET characteristic within any RC-IGBT type hybrid embodiment.

With respect to the RC-IGBT type structure the new lateral injector allows much reduced on state loss during the MOSFET conduction mode as the full drain contact area is exposed to direct electron flow, not partially obscured by any vertically placed P+ type injector (IGBT collector) region which causes congestion of the electron flow path and hence higher drift resistance. The complexity and cost of fabrication is also reduced when using a laterally placed injector in comparison to the RC-IGBT type structure as it requires no masked back side wafer stages. The backside processed RC-IGBT device also uses thinned, non epitaxial (float zone grown), silicon wafers, even though it is possible to thin a substrate to achieve 600 V BV the performance of any MOSFET fabricated within such a simple IGBT type structure will never be as good as a charge balanced MOSFET. Hence, to achieve hybrid performance separate die once again become attractive. The use of a thinned substrate wafer however, does provide a thermal advantage to both types.

Integration of the hybrid injector

The novel injector is a merged high barrier height Schottky diode and P type injector. To form the example hybrid device from a standard unipolar VDMOSFET the injector has been placed laterally adjacent to the channel as shown in fig 2a. The lateral injector forms Anode 2 which is connected directly to Anode 1 (or VDMOSFET Drain). Previous works have included a Schottky contact to form a Schottky Injected Field Effect Transistor (SINFET), Sin[13],[14]. This however, used a low barrier height ($\phi_B=0.4$ eV), aluminum based, Schottky to N- contact. The low barrier height was used to maximize hole injection from the metal emitter to N-Epi drift region. The SINFET however, required a floating potential on the P type substrate to avoid high Anode to substrate (collector) leakage currents (via the resulting vertical metal emitter PNP transistor). Any junction isolation obviously adds thermal resistance to the heat flow path, but the idea may lend itself to some membrane or oxide isolated structures. The benefits of the new merged injector structure are that no non-gated current is suffered via the Schottky contact as it is at the same potential as Anode 1. The heat flow of the resultant hybrid is via the N+ substrate which also forms the electrical connection to the positive supply rail ($+V_{AK}$).

In the new laterally placed minority carrier injector a high barrier height Schottky is used, as could be achieved using a platinum silicide (PtSi) contact as described by Zhang[15]. This provides a work function of around 5.2 to 5.8 eV, resulting in a barrier height (ϕ_B) > 0.84 eV, Ottaviani[16]. As a result of integrating the merged minority carrier injector into the VDMOSFET structure a lateral PNP bipolar device is formed as shown in figure 2b.

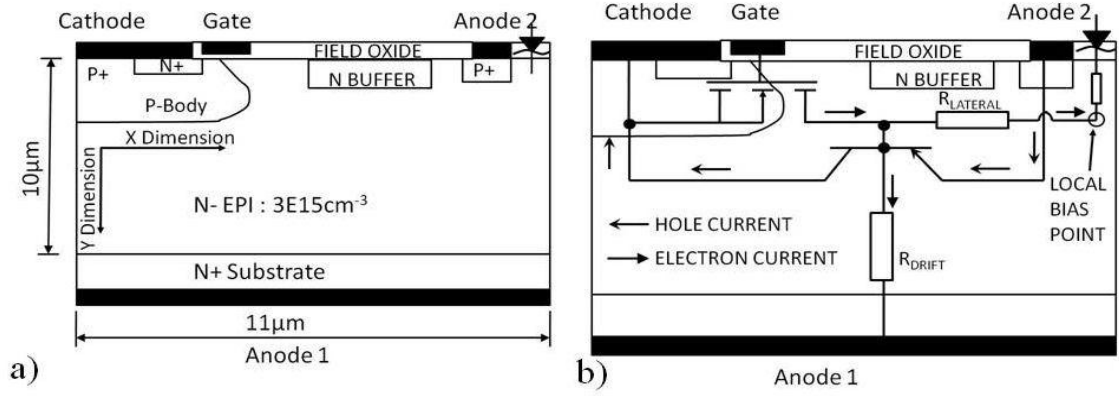


Fig. 2: a) Embodiment of the new Schottky biased injector into a standard VDMOSFET (forming Anode 2 of the hybrid), b) Key elements of the Hybrid device shown as an overlay on to the as modeled half cell.

The key elements of the hybrid device in terms of the equivalent schematic have been shown in figure 2b as an overlay of the half cell model. Once the MOS channel is inverted (Gate to Cathode Voltage, $V_{\text{GK}} > V_{\text{TH}}$), electrons are enabled to flow into the drift region from the Cathode via a resistive network made up of R_{DRIFT} and R_{LATERAL} splitting the electron current in a ratio of approximately 10:1 respectively. The resistive element Ohmic values are adjusted by increasing or decreasing the lateral or vertical distance. Anode 1 and Anode 2 are connected to $+V_{\text{AK}}$. Initially electrons only flow to Anode 1 as the high barrier height Schottky and merged P+ to N-type epitaxial layer (N-Epi) potential barrier prevents any electron flow to Anode 2.

Operation of the Anode 2 injector at 300 K is as follows. With increasing V_{GK} levels increased electron charge builds up at the local bias point. This point eventually reaches a charge level at which the Schottky barrier height is overcome (at $V_{\text{AK}} > 1.7 \text{ V}$) and a thermionic emission current flows towards Anode 2, as indicated by the electron concentration directly under the Schottky junction as shown in figure 3a. The forward voltage drop across the Schottky element ensures that the local bias point is now biased at approximately 0.7 V lower potential than the Anode 2 applied bias, which is a sufficient to forward bias the P+ injector of Anode 2 as indicated by the electron quasi Fermi potential directly under the P+ emitter of Anode 2, as shown in figure 3b. The electron flow to Anode 2 therefore now allows holes to be injected into the drift region requiring further increase in the electron concentration over and above the doping concentration, as shown in figure 3a. This gives a reduction in MOSFET drift region resistance from approximately 15.5 k Ω to 840 Ω and the PNP bipolar base is now biased on so electrons from the channel provide the base drive current. Further increase in V_{GK} provides higher base drive until the channel saturates (or pinches off). The Schottky element maintains the PNP emitter–base bias despite the lower resistance drift region resulting from the injection start up, without this fixed bias element any injection would cease due to the de-biasing of the Anode 2 P+ to N-Epi (PNP emitter to base) junction.

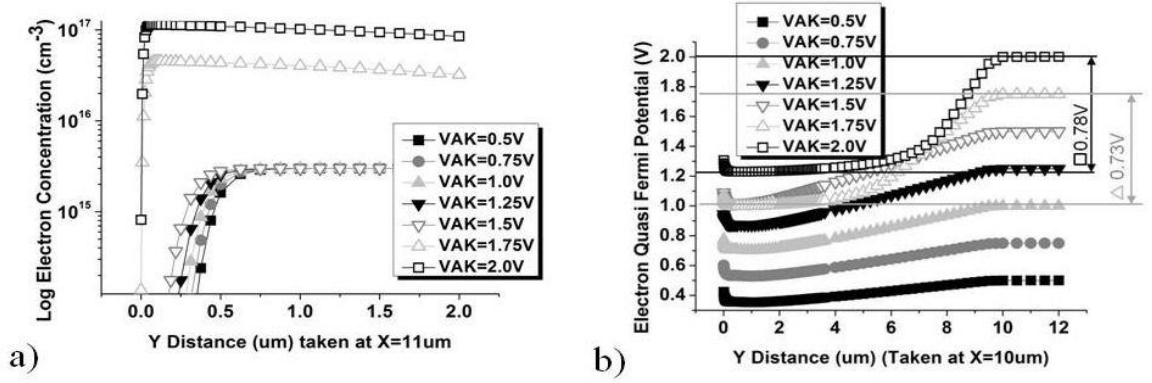


Fig. 3: a) Electron Concentration (at 300 K) directly under the Schottky junction, extending 2 μm in to the N-Epi layer. b) The Electron Quasi Fermi Potential (at 300 K) directly under the P+ emitter of Anode 2 extending 2μm into the N+ substrate

Description of compared device structures

The half cell structures of the non injected VDMOSFET and IGBT used to provide a performance comparison with the injected VDMOSFET (hybrid) device is shown in figure 4. Within all three models the identical P-body and channel design was incorporated. A retrograde P-body as described by Sze[17] was utilised. The effect of this is to minimize V_{TH} and greatly delay the onset of channel pinch-off in terms of V_{AK} relative to V_{GK} and V_{TH} .

Using an identical drift region doping of $3 \times 10^{15} \text{ cm}^{-3}$ the drift region length of the VDMOSFET and IGBT were adjusted to obtain approximately identical BV as achieved by the hybrid, at 300 Kelvin, while minimizing on state loss. The resultant drift region length is shown in figure 4. The drift region of the MOSFET was reduced relative to the IGBT because the MOSFET on state resistance (R_{AKon}) increases with drift length, whereas the IGBT on state loss is less sensitive to drift length, but has two depletion regions to consider. With $V_{GK}=0V$, and increasing V_{AK} one depletion region extends from the P-body to N-Epi junction (IGBT emitter to base) and the other forms at the P+ substrate to N-Epi (IGBT collector-base). A larger IGBT drift region prevents the extent of the depletion regions from reducing the neutral (or space charge) region, to the point where Cathode to Anode punch-through occurs. The substrate doping of the IGBT type was P+ ($1 \times 10^{20} \text{ cm}^{-3}$) to match that of the lateral injector doping in the hybrid.

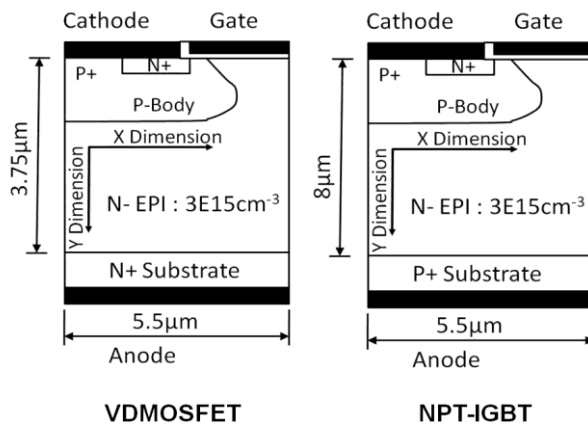


Fig. 4: Half cell schematics of the VDMOSFET and IGBT used as comparison.

Compared hybrid performance

To enable direct comparison over temperature a thinned silicon wafer substrate, equivalent to 120 μm thick, was added to all the half cell models shown in figure 2a and fig 4 by specifying a thermal resistance of $1 \times 10^5 \text{ K} \cdot \mu\text{m}/\text{W}$ from the Anode 1 contact. Anode 1 was declared as the thermal heat sink contact. The mobility was set to “Analytic” within the model to enable a concentration and temperature dependant calculation. The lattice temperature module was enabled which ensured that the simulation was completed for Poisson, continuity and lattice temperature. A comparison of blocking capability, forward conduction performance and switching performance was completed.

Blocking capability

To assess the blocking capability, each of the compared devices was simulated using a standardised program at an ambient heat-sink temperature of 300 K and 400 K with $V_{\text{GK}}=0 \text{ V}$, stepping V_{AK} in 1 V increments until conduction was evident. A direct comparison of the BV and leakage current achieved by each device is shown in figure 5a. Effectively the maximum BV that the hybrid device is capable of in silicon without the use of a charge balanced structure is limited by the radius of curvature of the P-body as the use of the lateral injector structure prevents shielding from the normally adjacent P-body of the neighbouring MOSFET cell.

With reference to figure 5a, the increased leakage current of the hybrid as compared to the VDMOSFET at 400 K is due to the extent of the lateral PNP collector–base (Cathode to N-Epi) depletion region. With increasing V_{AK} the depletion region extends from the Cathode towards Anode 2 (the injector). Prior to collector-base junction avalanche the effective PNP base width relative to Anode 2 (emitter) is continually reducing, the distance carriers diffuse across is therefore also decreasing. The reduction in the traversed distance together with the higher generation rate occurring within a larger depletion region extent forms a cumulative effect for increased leakage current with increased levels of forward voltage drop (V_{AK}).

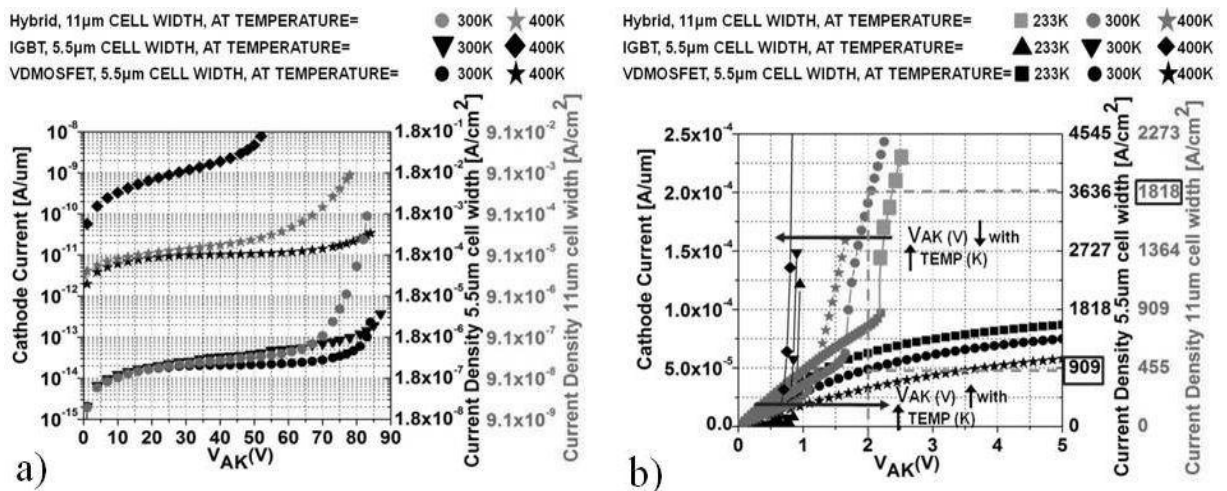


Fig 5: a) Direct comparison of Blocking Voltage and leakage current (Log_{10}) with $V_{\text{GK}}=0 \text{ V}$ at 300 and 400 Kelvin for the IGBT, VDMOSFET and hybrid device. b) A direct dc characteristic comparison of the same three device types under the same temperature conditions with $V_{\text{AK}}=2 \text{ V}$, $V_{\text{GK}}=20 \text{ V}$.

Forward conduction

To model the forward conduction performance over temperature under worst case conditions the carrier lifetimes were set to $1\mu\text{s}$ within each model. A direct comparison of the dc characteristics, at $V_{GK}=20\text{ V}$, $V_{AK}=2\text{ V}$, with ambient heat-sink temperatures set to 233 K , 300 K and 400 K is shown in fig 5b. The hybrid clearly demonstrates a current density of 2 times that of the VDMOSFET at $V_{AK}=2\text{ V}$, 300 K . The VDMOSFET and the hybrid conducting in the MOSFET (non-injected) state both demonstrate increased voltage drop with increasing temperature. Conversely, the injected hybrid and the IGBT both display a reduction in the on state voltage with increased temperature. However, at 300 K the start up of injection within the hybrid is 0.8V higher (in terms of V_{AK}) than the IGBT, whereas, at 400 K the onset of injection within the hybrid is only 0.4V higher as shown in figure 5b. At 400 K the reduction in V_{AK} at which injection occurs is due to the fact that the potential barrier between the P+ injector and N-Epi of the hybrid emitter is much lower at higher temperature allowing electrons to cross into the P+ injector and hence the injection of minority carriers begins earlier in terms of forward volt drop (V_{AK}). Figure 6a shows the plots of RAK_{ONSP} and area of the compared devices relative to V_{AK} at 400 K . At $V_{AK} = 1.18\text{ V}$ both RAK_{ONSP} and area plots can be seen to cross over those of the VDMOSFET once bipolar conduction starts.

Upon comparison of the hybrid with the IGBT in figure 5b (and fig. 6a) the rate of increase of current (or decrease of RAK_{ONSP}) with Anode Cathode Voltage (V_{AK}) of the hybrid can clearly be seen to be less than that of the conventional IGBT. This is due to the electrons from the channel in the hybrid are not only supplying PNP base drive and base to emitter electron current as per the IGBT, but also providing a MOSFET drain current. The hybrid device would therefore benefit from optimization of the PNP gain in order to maximize the minority carrier injection for a given base to emitter electron current.

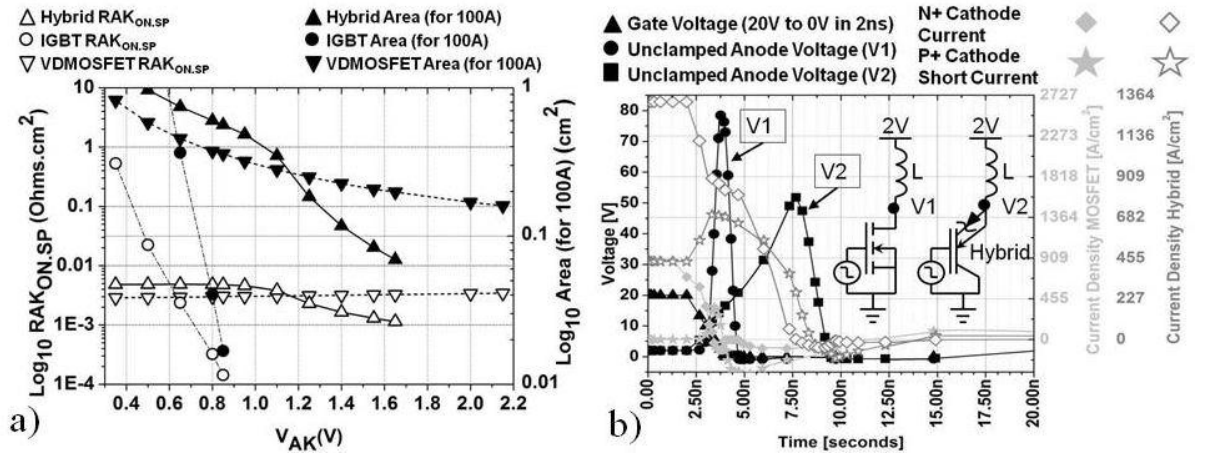


Fig. 6: a) A direct comparison of the compared devices in terms of specific on state resistance and active area required to conduct 100 A, with $V_{GK}=20\text{ V}$ at 400 K , b) Switching performance comparison of the hybrid and MOSFET at 300 K .

Switching capability

Switching performance of the comparison device models was completed at 300 K with carrier lifetime set to $100\mu\text{s}$ to provide a worst case scenario in silicon. All other parameters were set as previously described except that the Cathode on each model was separated into a P+ Cathode short and N+ Cathode contact. The circuit was designed with reference to JEDEC standard on

unclamped inductive switching[18]. The gate pulse was set to 20V initially with a delay of 2 ns prior to a 2 ns ramp down to 0 V. A 900 H pure inductive load was used in the switching circuit. This unfeasible size in reality is required within the simulator as the inductor only has 2 ns to charge from a 2 V supply and the actual inductor size is factored by the modelled channel width, in this case 1×10^{-6} m.

The switching performance results of the MOSFET and hybrid are directly compared in fig 6b. The IGBT has been omitted as the timeline would need to stretch out to 10 μ s to reach the 10 % point of the original Anode current. The comparative turn-off energy (avalanche energy for the MOSFET) is shown in table I, within which the hybrid is seen to be much reduced when compared to an IGBT.

	VDMOSFET	IGBT	Hybrid
Turn-off energy (J/cm ²)	7.55×10^{-5}	8.72×10^{-3}	1.26×10^{-4}

Table I: Comparative turn off energy for hybrid & IGBT with MOSFET avalanche energy

MOSFET inductive switching is well documented, see Baliga[19], however with reference to fig 6b the hybrid switching characteristic is different. As can be seen despite a high minority carrier concentration, the hybrid, unlike an IGBT, is not subject to dynamic latch up. Upon ramp down of the gate the electron current via the N+ Cathode contact immediately begins to fall, conversely, driven by the inductor, the hole current increases to compensate. As soon as the $\text{Gate} \leq V_{\text{TH}}$ ($=5.5$ V), the hole current begins to decrease, maximum hole current therefore occurs at $T=3.3$ ns. Sufficient hole current exists from $T=2.5$ ns to develop a voltage drop across the N+ Cathode length in excess of 0.7 V which biases on the parasitic NPN transistor. This has the effect of maintaining hole current via the PNP for a short duration, but NPN conduction however, is not sustained as the electron current continues to falls due to the influence of Anode 1(VDMOSFET Drain). Once the resulting PNP base bias is <0.7 V the PNP shuts off hole supply and hence the NPN no longer has sufficient base bias to conduct. Indeed the conduction of the NPN is a benefit to the hybrid as the current flow allows the device to ‘self clamp’ the inductive load, thus preventing avalanche within the device. The switching times of the hybrid are very similar the MOSFET. Equilibrium is established for both devices within 30 ns. Thus, the hybrid is suitable to switch inductive loads in comparable times to a VDMOSFET.

The effects of the stray capacitance on switching of the hybrid have been included in the models used, such as input capacitance (Gate –Cathode + Miller), output capacitance (Anode to Cathode) and reverse transfer capacitance (Miller). The capacitance due to any wire bonds was not included, but is small (fF) which offers relatively little affect at low kHz switching frequencies (up to 100 kHz). Similarly, no inductance was included in either the Cathode, Gate or Anode 2 contact to replicate within the model the inductance of the required wire bonds. Such inductance is not typically quoted by packaged device manufacturers as the effect of any ‘in package’ inductance is minuscule compared to the interconnecting circuit.

Concept exploitation

The Schottky biased minority carrier injector, as demonstrated herein as an injected hybrid as compared to a simple VDMOSFET structure, has been proven via simulation to provide

significant minority carrier injection. As a result, the injected hybrid device demonstrated a significant reduction in specific on state resistance (RAK_{ONSP}) when operating in the bipolar mode as compared to the non injected VDMOSFET of the same Blocking Voltage as shown in figure 6a. The hybrid is not intended to compete with IGBTs where they operate well, it is intended as extension of the capability of MOSFETs, it is of no surprise therefore that the comparison IGBT demonstrates lowest loss and lowest area required in order to conduct 100A. The hybrid does however, demonstrate that through the use of Schottky biased merged injector within a VDMOSFET structure a large reduction in RAK_{ONSP} is achievable under surge current or over voltage conditions and yet as described previously the switching time of the hybrid in bipolar mode compares favorably with a unipolar VDMOSFET and demonstrates much reduced turn off energy when compared to an IGBT. The only detriment to using the injector is that as shown in figure 6a the area required to conduct 100 A in unipolar mode is increased over that of the standard VDMOSFET of the same blocking voltage, due to the laterally placed injector. In applications where the safe conduction of surge current is key to system reliability then the resultant silicon area is less important commercially as compared to increased reliability. The example hybrid therefore demonstrates the potential to open up a new class of fast switching bipolar devices to augment the MOSFET device family capabilities.

To exploit the new injector concept the next stage of development will be to demonstrate the usage of the charge balance concept now commonly used in commercially available MOSFET devices. As regards a potential silicon carbide VDMOSFET implementation of the laterally injected hybrid, it is expected that because of the higher dielectric strength relative to silicon (approximately 10 times higher), then for similar cell dimensions, as those shown in figure 2a, a silicon carbide variant could achieve a Blocking Voltage of approximately 1 kV with much reduced $R_{(ON)}$ associated with SiC. The hybrid device proposed would provide MOS gate controlled bipolar conduction on an N+ substrate, this is significant since n-channel IGBTs require a P+ substrate and these are not available in SiC, therefore alternative methods of fabricating an IGBT in SiC have been demonstrated by Xiaokun[20]. Unfortunately, the continuing MOS channel mobility issues of silicon carbide VDMOSFET structures may delay any successful implementation of the injected hybrid design within that material.

Applications that may benefit from the hybrid device in the region of 600V are possibly to replace contactors in electric vehicles and high switching speed inverters. The advantages of using a hybrid MOSFET-IGBT within an inverter are well described by Selamogullari[21].

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Appendix 2 | Optimisation of VDMOSFET for lowest on state resistance

A2.0 Introduction

This appendix contains any data cross checks related to the optimisation of the VDMOSFET for lowest static loss (chapter 3 of this thesis).

A2.1 Calculation of V_{TH} using diffused P-body design

Using the original as optimised (diffused) P-body design the ideal V_{TH} is calculated as follows:-

Using equation 3.13 of chapter 3 then

$$V_{TH} = \frac{\sqrt{2K_s \epsilon_o q N_a 2\psi_B}}{C_{OX}} + 2\psi_B \quad (\text{V}) \quad (\text{A2.1.1})$$

$$\psi_s(\text{stronginv}) = 2\psi_B = \frac{2kT}{q} \ln\left(\frac{N_a}{n_i}\right) \quad (\text{A2.1.2})$$

Where : $N_a = 3 \times 10^{17} \text{ cm}^{-3}$, $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$, $q = 1.6 \times 10^{-19} \text{ C}$, $kT/q = 25.4 \times 10^{-3} \text{ V}$

$$2\psi_B = \frac{2kT}{q} \ln\left(\frac{3E17}{1.45E10}\right) \quad (\text{A2.1.3})$$

$$2\psi_B = 0.869 \text{ V} \quad (\text{A2.1.4})$$

Now,

$$C_{OX} = \frac{K_o \epsilon_o}{t_{OX}} \quad (\text{F}) \quad (\text{A2.1.5})$$

Where: $t_{ox} = 0.2 \times 10^{-4} \text{ cm}$, $\epsilon_o = 8.854 \times 10^{-14} \text{ F/cm}$, $K_o = 3.9$

$$C_{OX} = \frac{3.9 * 8.854E - 14}{0.2E - 4} \quad (\text{A2.1.6})$$

$$C_{OX} = 1.72E - 8 \text{ F/cm}^2 \quad (\text{A2.1.7})$$

Using equation A2.1.1:-

$$V_{TH} = \frac{\sqrt{2K_S \epsilon_O q N_a 2\psi_B}}{C_{OX}} + 2\psi_B \text{ (V)}$$

Where: $K_S = 11.8$

$$V_{TH} = \frac{\sqrt{2 \times 11.8 \times 8.854E - 14 \times 1.6E - 19 \times 3E17 \times 0.869}}{1.72E - 8} + 0.869 \text{ (V)} \quad (\text{A2.1.8})$$

$$V_{TH} = \frac{2.952E - 7}{1.72E - 8} + 0.869 \text{ (V)} \quad (\text{A2.1.9})$$

$$V_{TH} = 18.03 \text{ V} \quad (\text{A2.1.10})$$

A2.2 Calculation of V_{TH} using retrograde P-body design

For the retrograde P-body with reduced N_a doping at the silicon surface

$$V_{TH} = \frac{\sqrt{2K_S \epsilon_O q N_a 2\psi_B}}{C_{OX}} + 2\psi_B \text{ (V)} \quad (\text{A2.2.1})$$

$$\psi_s(\text{stronginv}) = 2\psi_B = \frac{2kT}{q} \ln\left(\frac{N_a}{n_i}\right) \quad (\text{A2.2.2})$$

Where : $N_a = 4 \times 10^{16} \text{ cm}^{-3}$, $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$, $q = 1.6 \times 10^{-19} \text{ C}$, $kT/q = 25.4 \times 10^{-3} \text{ V}$

$$2\psi_B = \frac{2kT}{q} \ln\left(\frac{4E16}{1.45E10}\right) \quad (\text{A2.2.3})$$

$$2\psi_B = 0.765 \text{ V} \quad (\text{A2.2.4})$$

Now,

$$C_{OX} = \frac{K_O \epsilon_O}{t_{OX}} \text{ (F)} \quad (\text{A2.2.5})$$

Where: $t_{ox} = 0.2 \times 10^{-4} \text{ cm}$, $\epsilon_O = 8.854 \times 10^{-14} \text{ F/cm}$, $K_O = 3.9$

$$C_{OX} = \frac{3.9 \times 8.854E - 14}{0.2E - 4} \quad (\text{A2.2.6})$$

$$C_{OX} = 1.72E - 8 \text{ F/cm}^2 \quad (\text{A2.2.7})$$

Using equation A2.1.1:-

$$V_{TH} = \frac{\sqrt{2K_S \epsilon_O q N_a 2\psi_B}}{C_{OX}} + 2\psi_B \text{ (V)}$$

Where: $K_S = 11.8$

$$V_{TH} = \frac{\sqrt{2 * 11.8 * 8.854E-14 * 1.6E-19 * 4E16 * 0.765}}{1.72E-8} + 0.765 \text{ (V)} \quad (\text{A2.2.8})$$

$$V_{TH} = \frac{1.011E-7}{1.72E-8} + 0.765 \text{ (V)} \quad (\text{A2.2.9})$$

$$V_{TH} = 6.64 \text{ V} \quad (\text{A2.2.10})$$

The use of the retrograde profile will therefore provide a calculated reduction in V_{TH} of 11.39

V, this ideal calculation does not take into account any factors influencing the flat band

voltage (V_{FB}).

Appendix 3 | Achieving bipolar conduction

A3.0 Introduction

This appendix contains any data cross checks related to the section describing methods of achieving bipolar conduction (chapter 4).

A3.1 Calculation of the built in potential of a P-N junction

The level of V_{BI} is dependent upon the relative doping of the P and N type regions as shown in equation A3.1.1.

$$V_{BI} = \frac{kT}{q} \ln \left(\frac{N_a N_d}{n_i^2} \right) \text{ (V)} \quad (\text{A3.1.1})$$

Using equation A4.1.1 with the Peak acceptor doping concentration of $N_a = 1 * 10^{20} \text{ cm}^{-3}$ and $N_d = 3 * 10^{15} \text{ cm}^{-3}$ then the V_{BI} can be calculated as follows:-

$$V_{BI} = 26E - 3 * \ln \left(\frac{1E20 * 3E15}{1E20} \right) \text{ (V)} \quad (\text{A3.1.2})$$
$$V_{BI} = 0.92 \text{ V}$$

Using equation A3.1.1 with the Peak acceptor doping concentration of $N_a = 1.15 * 10^{17} \text{ cm}^{-3}$ and $N_d = 3 * 10^{15} \text{ cm}^{-3}$ then the V_{BI} can be calculated as follows:-

$$V_{BI} = 26E - 3 * \ln \left(\frac{1.15E17 * 3E15}{1E20} \right) \text{ (V)} \quad (\text{A3.1.3})$$
$$V_{BI} = 0.75 \text{ V}$$

The value of V_{BI} can also be obtained by integrating the electric field, which in turn is the integral of charge. Alternatively, V_{BI} can be calculated using the intrinsic energy level on a band diagram as discussed by Parker[1], using illustration as shown in figure A3.1.1.

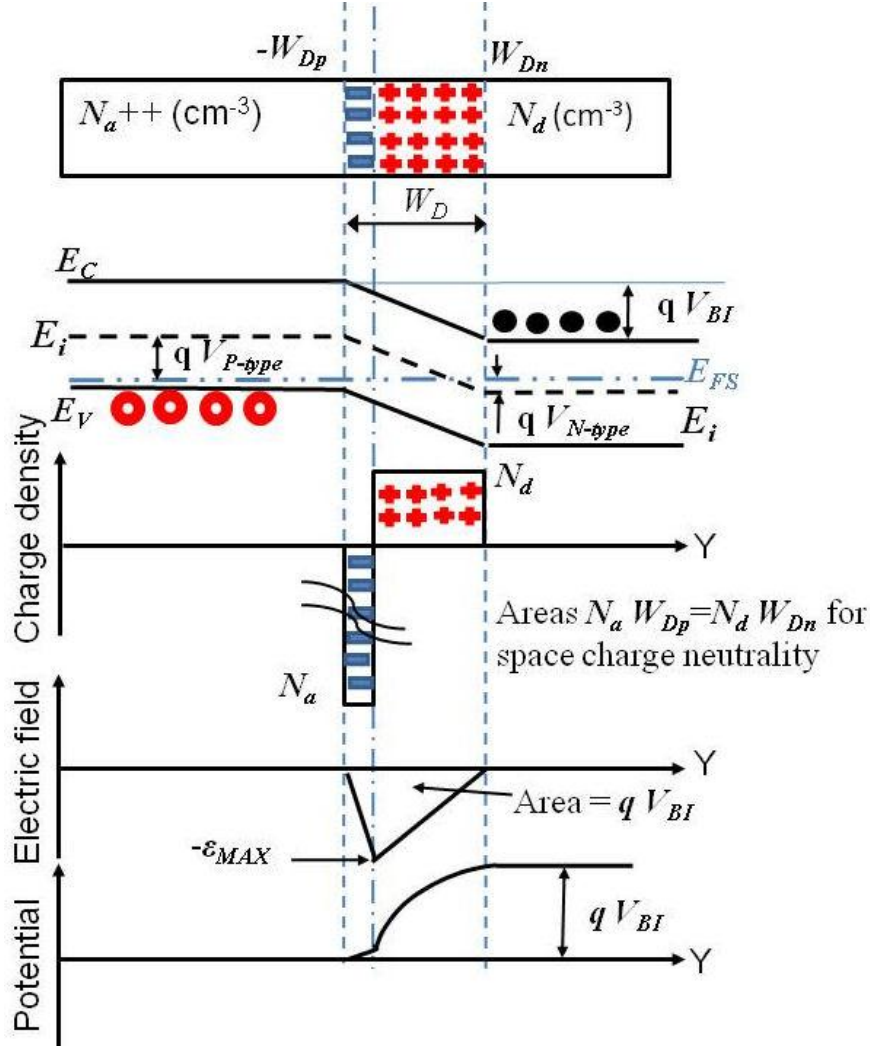


Figure A3.1.1. Band diagram, charge, electric field and potential of a generic P-N junction.

Where:

$$qV_{P-type} = -(E_i - E_{FS}) \quad (V)$$

$$qV_{N-type} = -(E_i - E_{FS}) \quad (V)$$

$$V_{BI} = V_{N-type} - V_{P-type} = \frac{q}{2K_s \epsilon_0} (N_a W_{Dp}^2 + N_d W_{Dn}^2) \quad (V) \quad (A3.1.4)$$

A3.2 Calculation of the saturation current (I_o) of a P-N junction

Calculation of the saturation current within the P-N junction diode can be calculated for the illustration shown in figure A3.2.1 as follows:-

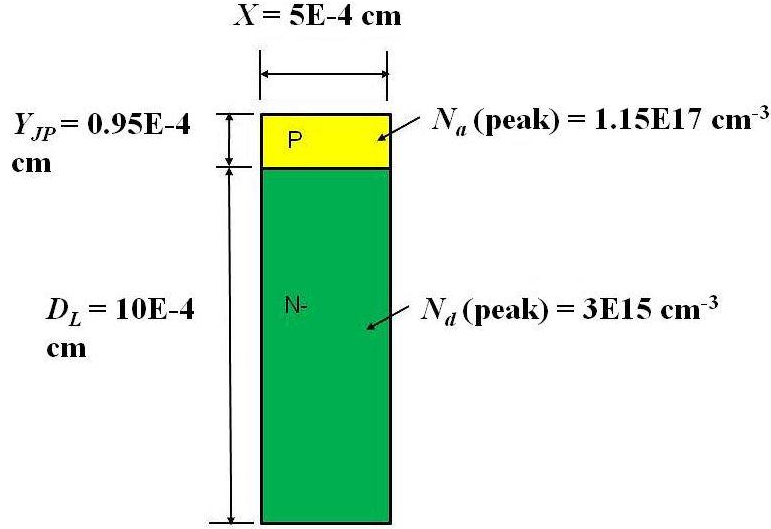


Figure A3.2.1. The one dimensional model for the Ion implanted profile as shown in figure 4.2 of chapter 4.

Parameters used for the calculation are shown below.

At $N_a = 1.15 \times 10^{17} \text{ cm}^{-3}$ then $\mu_p = 250 \text{ cm}^2/\text{V-s}$

At $N_d = 3 \times 10^{15} \text{ cm}^{-3}$ then $\mu_n = 1225 \text{ cm}^2/\text{V-s}$

$\tau_n = 1 \times 10^{-6} \text{ s}$

$\tau_p = 1 \times 10^{-6} \text{ s}$

$A = 0.95 \times 10^{-4} \times 5 \times 10^{-4} = 54.75 \times 10^{-8} \text{ cm}^2$

The above values were used in the simulation of the ion implanted P-N junction, theoretical calculation of the saturation current (I_o) is as follows:-

$$\frac{kT}{q} = 26E - 3 \quad (\text{V}) \quad (\text{A3.2.1})$$

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = \frac{kT}{q} \quad (\text{V}) \quad (\text{A3.2.2})$$

$$D_n = \frac{kT}{q} * \mu_n \text{ \& } D_p = \frac{kT}{q} * \mu_p \quad (\text{A3.2.3})$$

$$D_n = 26E - 3 * 1225 = 31.85 \text{ cm}^2/\text{s} \quad (\text{A3.2.4})$$

$$D_p = 26E - 3 * 250 = 6.5 \text{ cm}^2/\text{s} \quad (\text{A3.2.5})$$

$$L_p = \sqrt{(D_p \tau_p)} = \sqrt{(6.5 * 1E-6)} = 2.54E-3 \text{ cm} \quad (\text{A3.2.6})$$

$$L_n = \sqrt{(D_n \tau_n)} = \sqrt{(31.85 * 1E-6)} = 5.64E-3 \text{ cm} \quad (\text{A3.2.7})$$

L_n & $L_p \gg D_L$ & Y_{JP} therefore use the actual size of the modelled device in the calculation to obtain I_o .

From the ideal diode equation:-

$$I = I_o \left[\exp \frac{qV_{AK}}{kT} - 1 \right] (\text{A}) \quad (\text{A3.2.8})$$

$$I_o = \left[\left(qA * \frac{D_n}{Y_{JP}} * \frac{n_i^2}{N_a} \right) + \left(qA * \frac{D_p}{D_L} * \frac{n_i^2}{N_d} \right) \right] (\text{A}) \quad (\text{A3.2.9})$$

$$I_o = \left[\left(\frac{31.85}{0.95E-4} * \frac{1E20}{1.15E17} \right) + \left(\frac{6.5}{1E-4} * \frac{1E20}{3E15} \right) \right] * 8.809E-26 (\text{A})$$

$$I_o = 2.568E-18 \quad \text{A}/\mu\text{m}$$

A3.3 Calculation of the built in potential of Schottky junction

With use of the method as demonstrated by Pierret[2] the calculation of the built in potential can be calculated for a metal work function for Tungsten ($\Phi_M = 4.63 \text{ eV}$).

$$V_{BI} = \frac{1}{q} [\Phi_B - E_C - E_{FS}] (\text{V}) \quad (\text{A3.3.1})$$

Where:-

$$\Phi_B = \Phi_M - \chi = 4.63 - 4.05 = 0.58 (\text{eV}) \quad (\text{A3.3.2})$$

$$[E_C - E_{FS}] = \frac{E_G}{2} - kT * \ln \left(\frac{N_d}{n_i} \right) (\text{eV}) \quad (\text{A3.3.3})$$

$$[E_C - E_{FS}] = \frac{1.1}{2} - kT * \ln \left(\frac{3E15}{1E10} \right) (\text{eV}) \quad (\text{A3.3.4})$$

$$[E_C - E_{FS}] = 0.23 \text{ eV}$$

Using equation (A4.3.1) to obtain V_{BI}

$$V_{BI} = \frac{1}{q} [0.58 - 0.23] \text{ (V)} \quad (\text{A3.3.5})$$

$$V_{BI} = 0.35 \text{ V}$$

A3.4 References

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